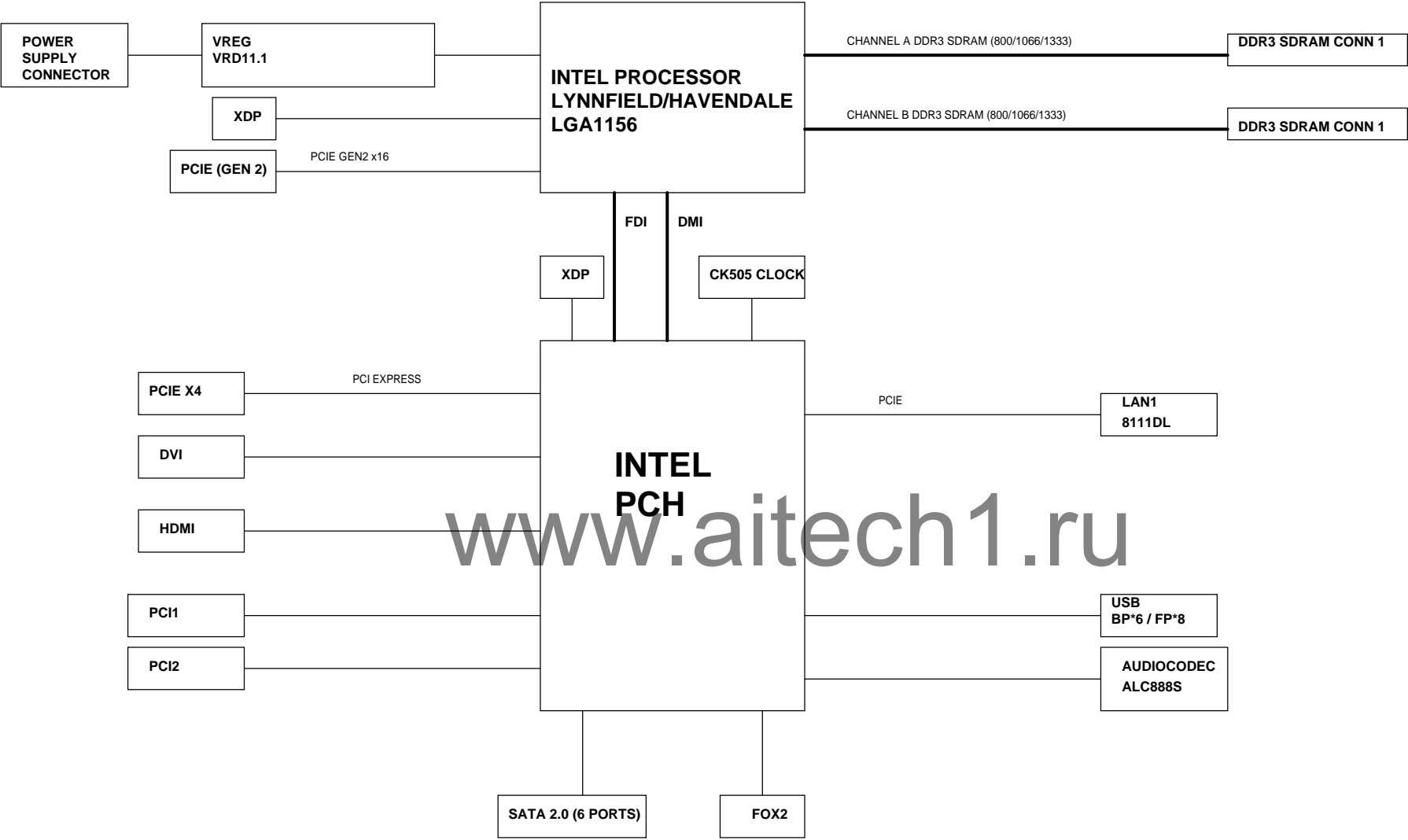
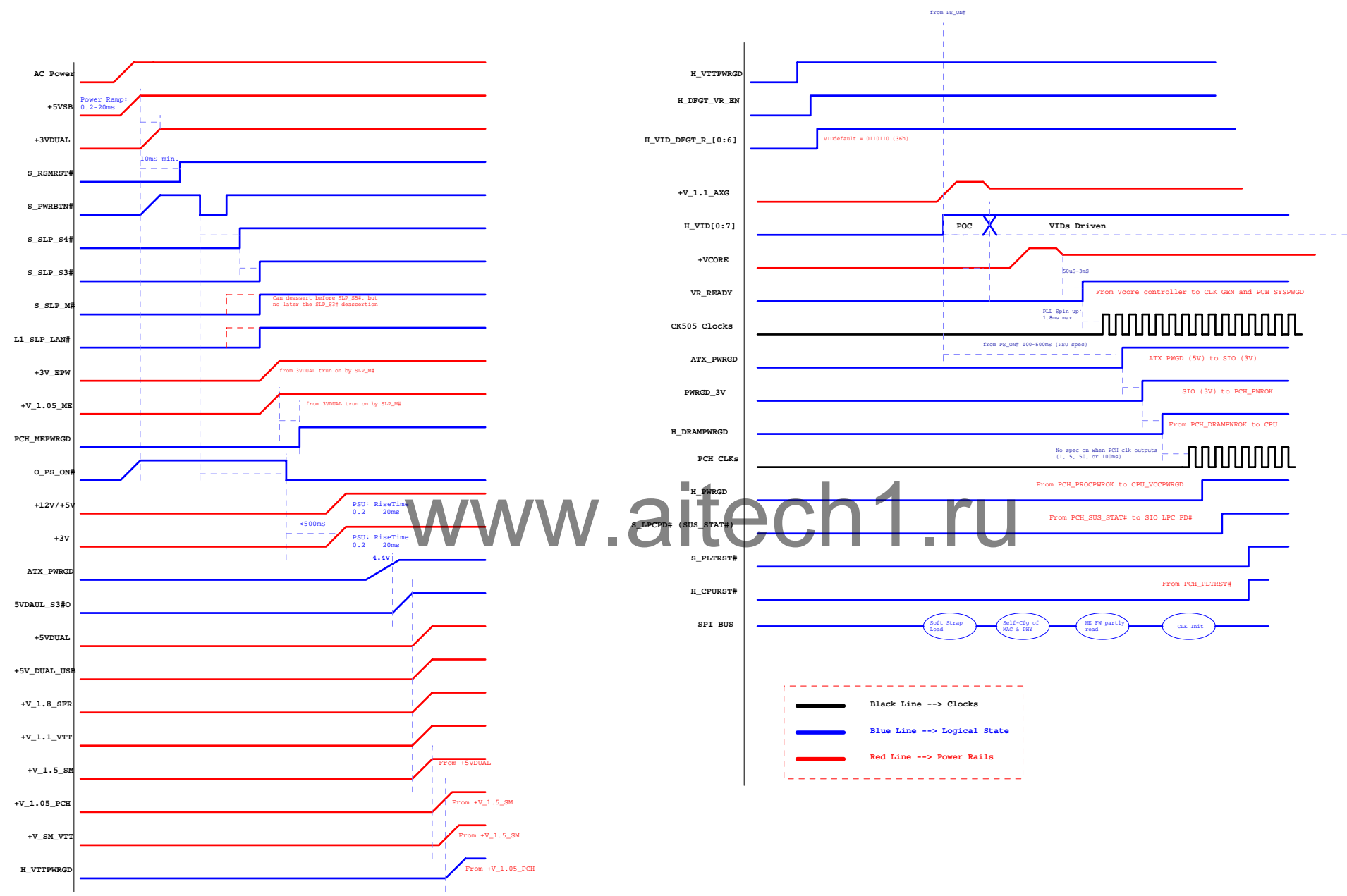


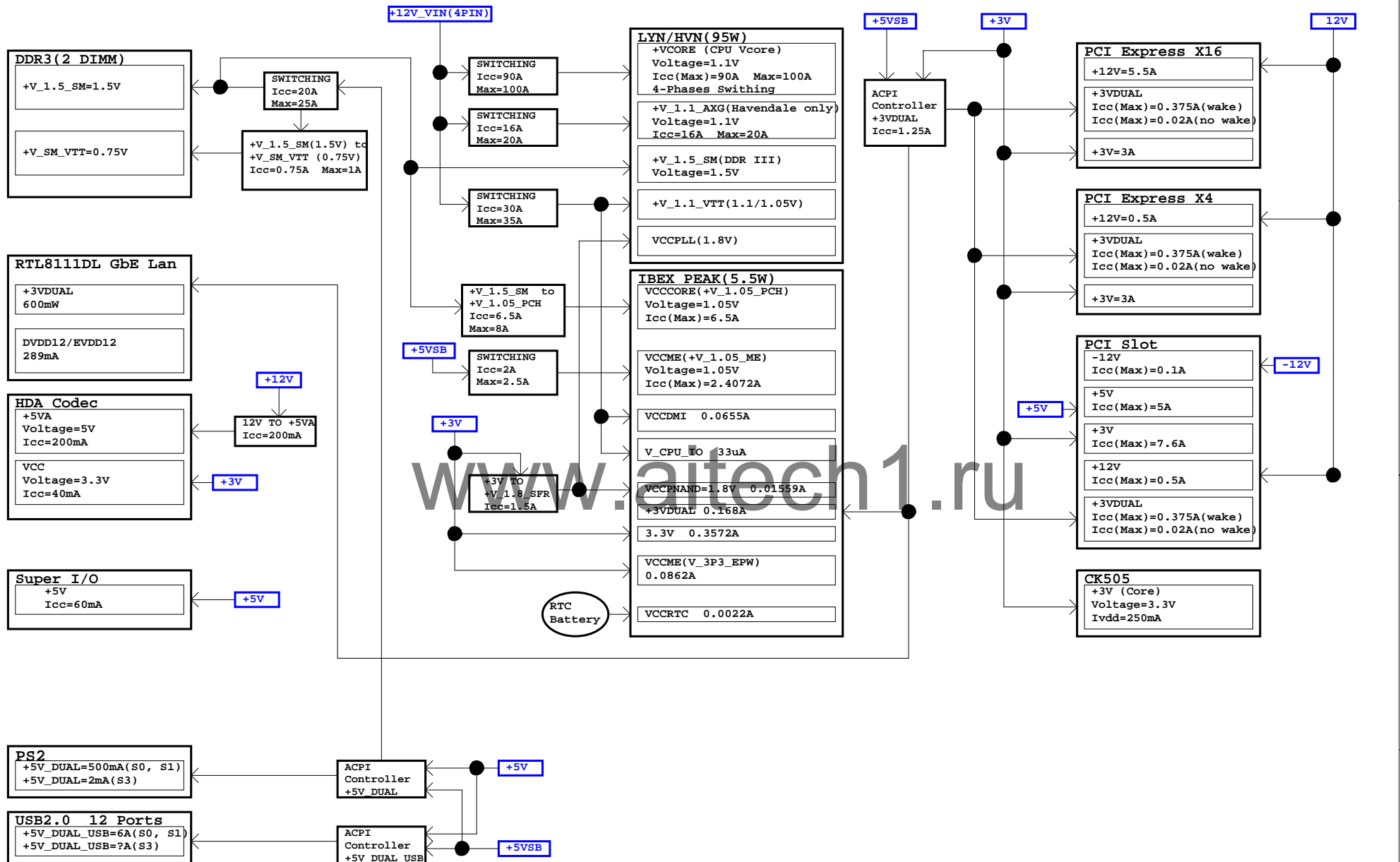
BLOCK DIAGRAM

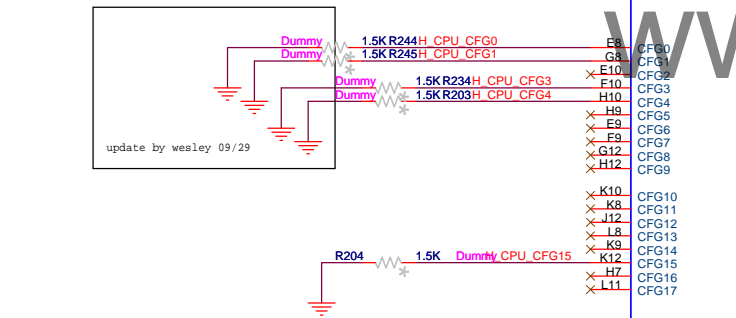
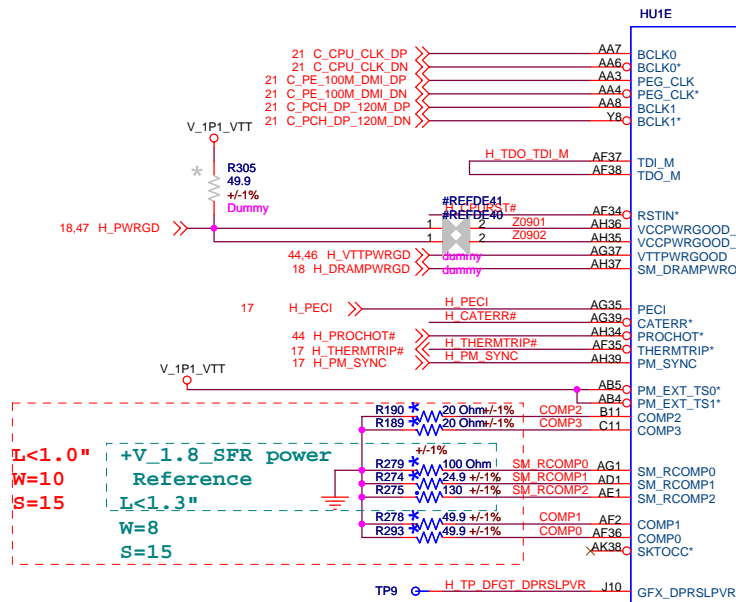


POWER ON SEQUENCE



POWER DELIVERY MAP





CFG Table

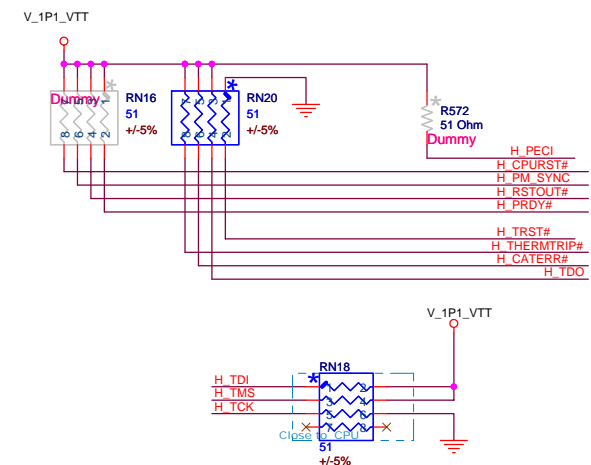
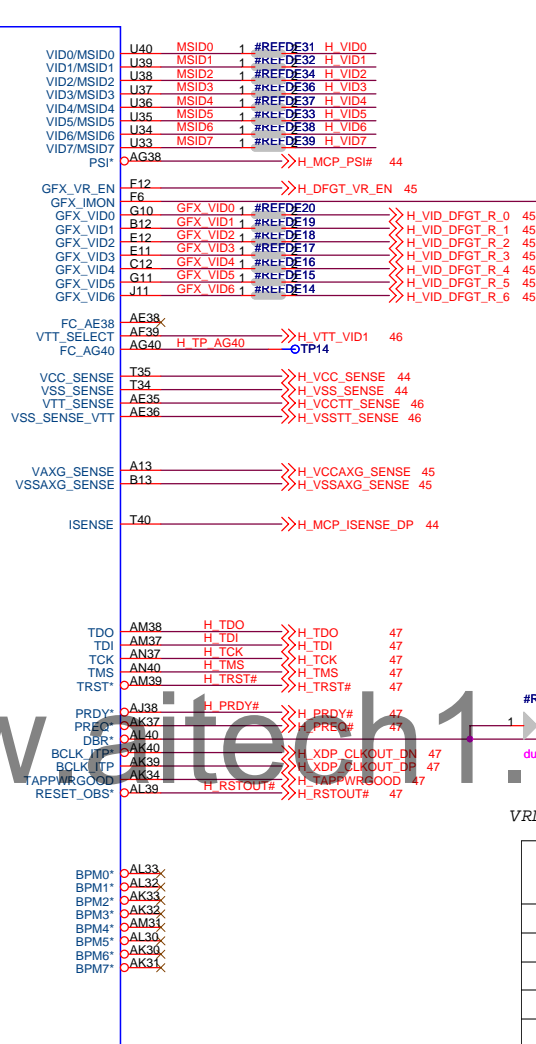
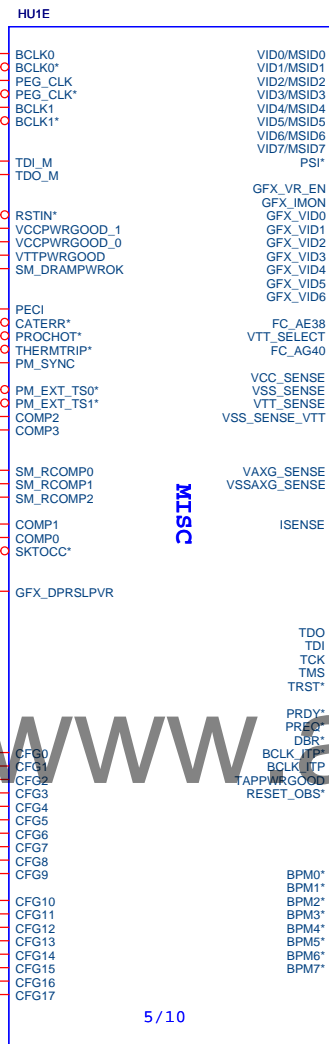
CFG	H / L	Description	
0	PEG Config Table	PEG SEL0	
1	PEG Config Table	PEG SEL1	
2	PEG Config Table	PEG SEL2	
3	Normal / Reverse	Lane Normal	
4	Disable / Enable	DP Presence	
5		RESERVED	
6		RESERVED	
7	ENGINEERING EXPERIMENT		
15	ENGINEERING EXPERIMENT		
CFG0..51 HAVE INTERNAL PULL-UP			
lynxfiel EDS Page 52, Wesley wang 033009			
SEL2	SEL1	SEL0	PCI-E Config
1	1	1	1 x 16
1	1	0	2 x 8

Power On Config

Function	Default
VID0	MSI0
VID1	MSI1
VID2	MSI2
VID3	IMON CONFIG0
VID4	IMON CONFIG1
VID5	IMON CONFIG2
VID6	RESERVED
VID7	VRD SELECT
PSI#	RESERVED

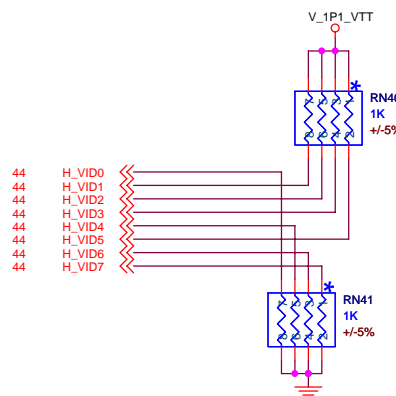
MISC

5/10



VRD design guide Page 43

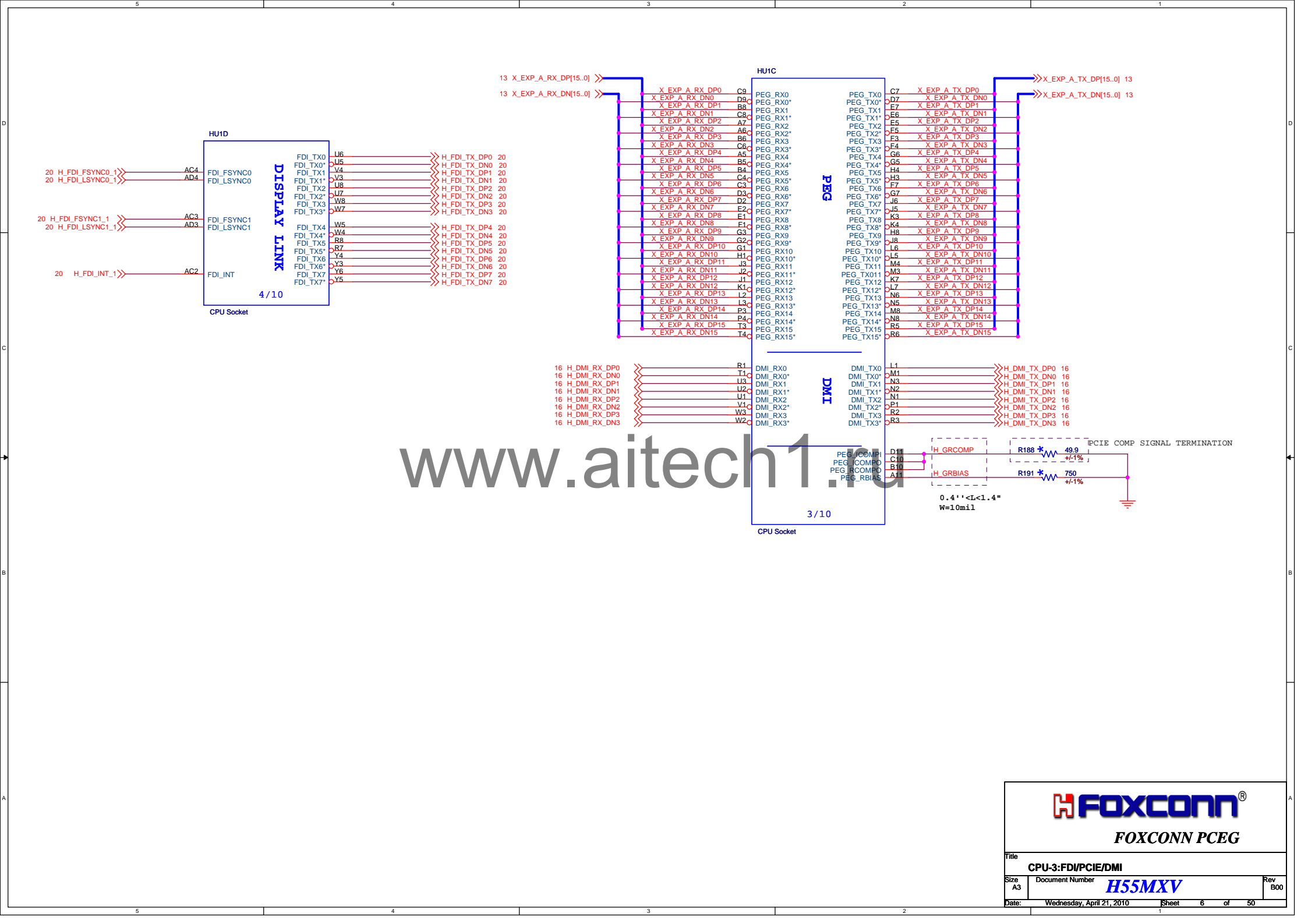
Processor Icc(max)	I _{MAX} Iout gain: 900 mV = I _{MAX}	POC Gain Setting VID3~5
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111



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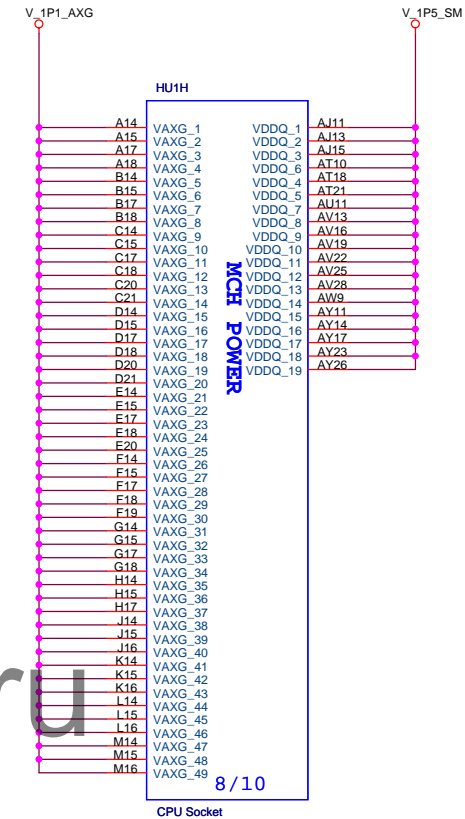
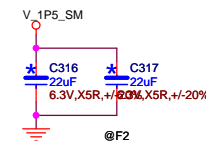
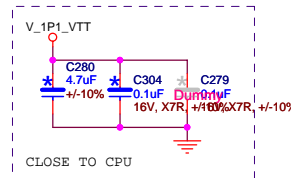
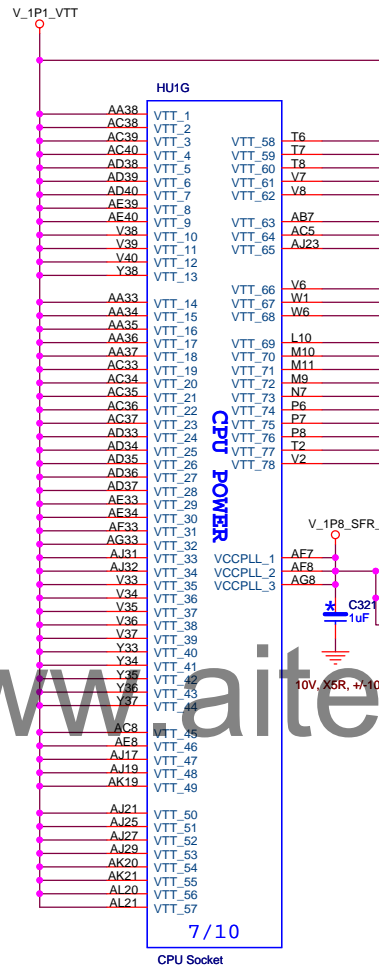
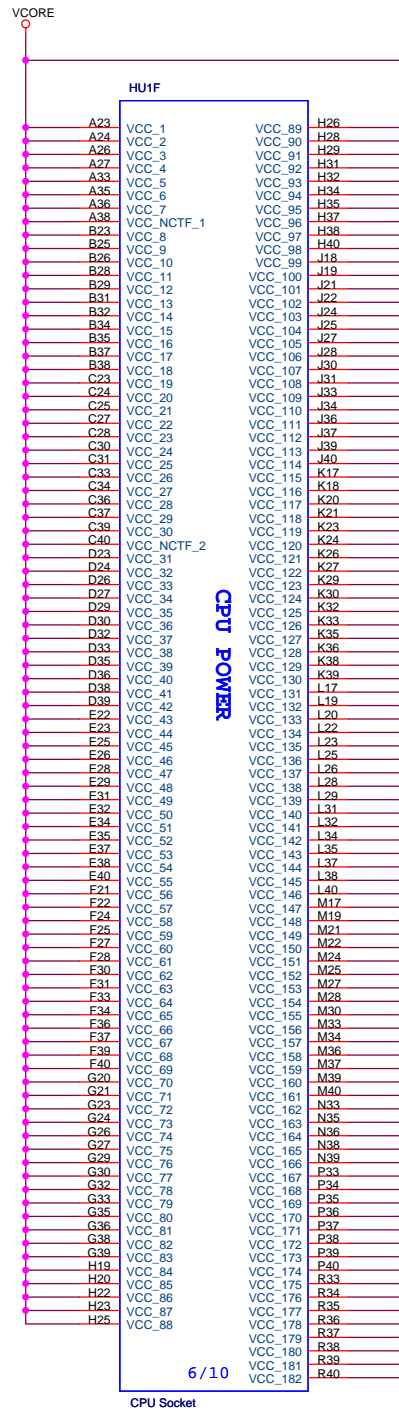
FOXCONN PCEG

Title			CPU-1:MISC
Size	A3	Document Number	H55MXV
Date:	Wednesday, April 21, 2010	Sheet	5 of 50



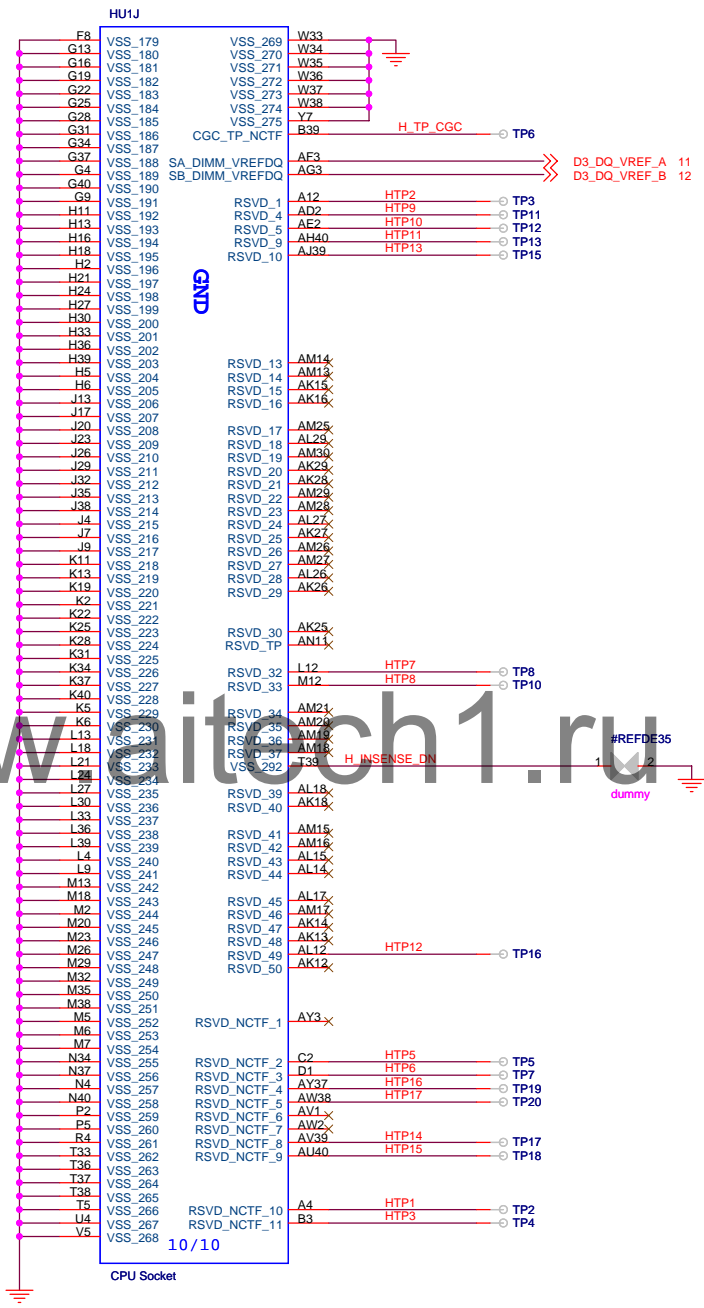
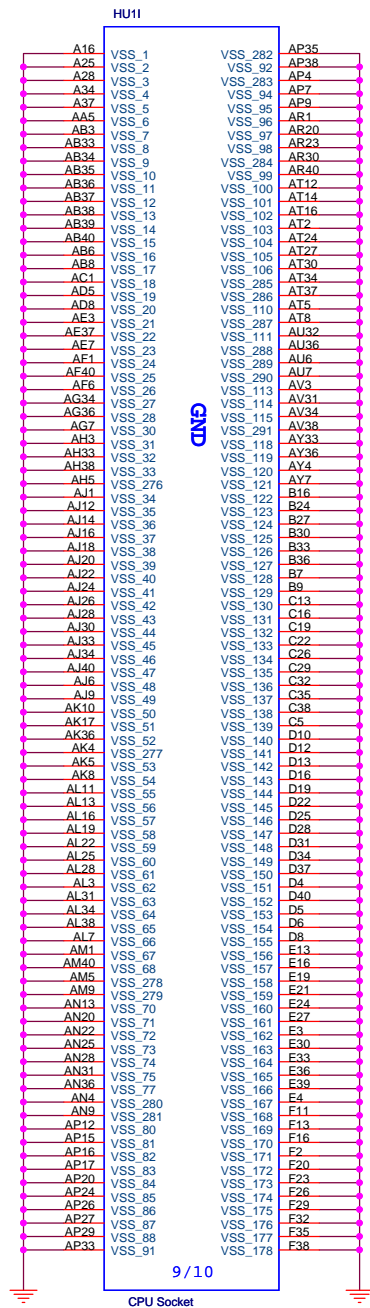
FOXCONN PCEG

Title			CPU-3:FDI/PCIE/DMI
Size	Document Number	H55MXV	
A3			
Date:	Wednesday, April 21, 2010	Sheet	6 of 50

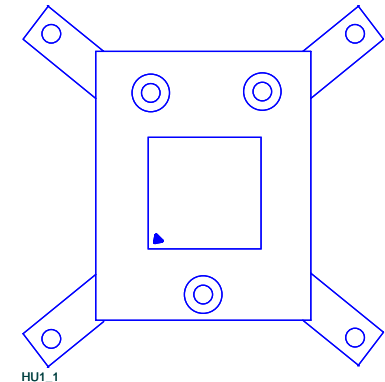


FOXCONN

FOXCONN PCEG



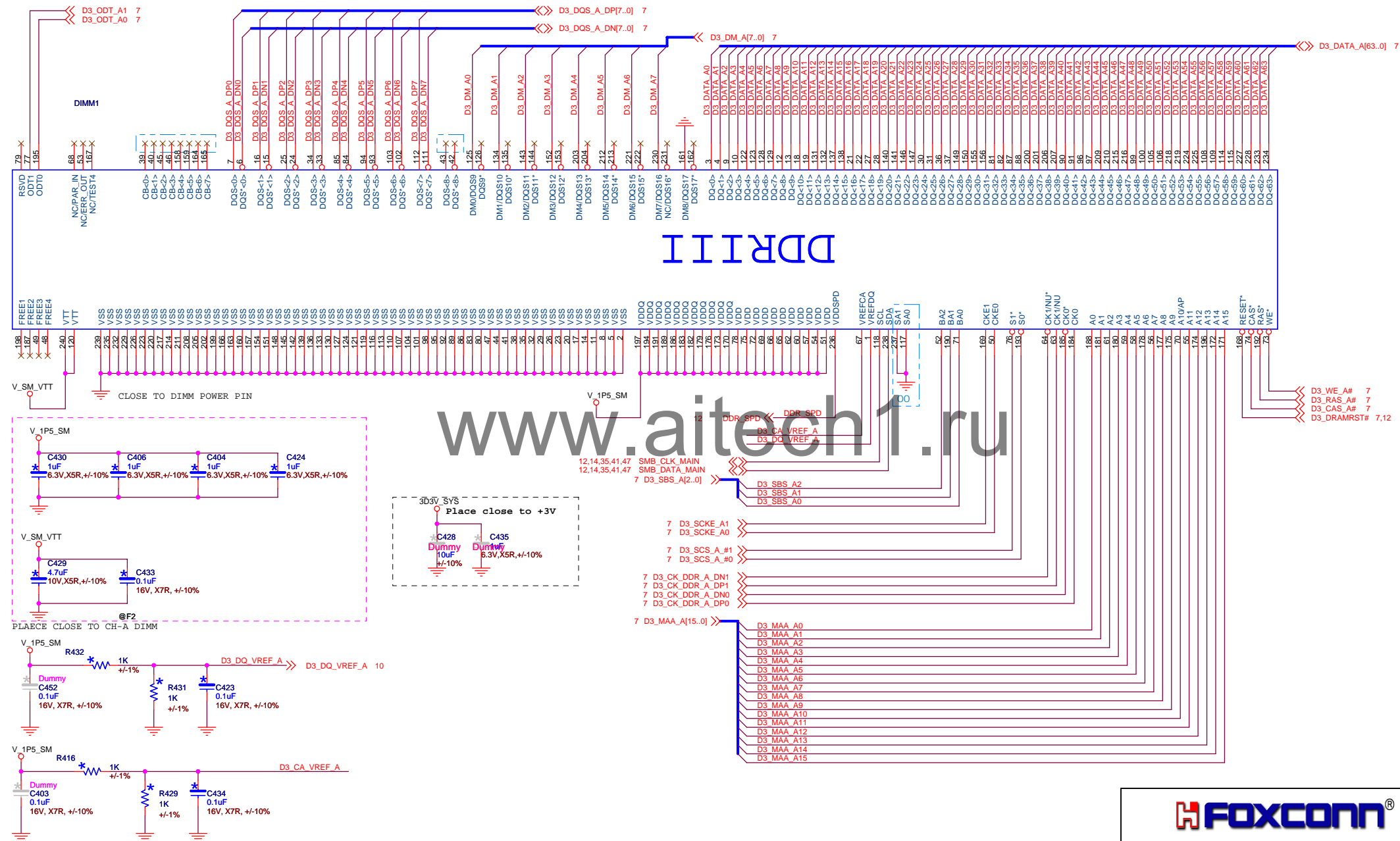
update by wesley 0715



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FOXCONN PCEG

Title			CPU-7:GND
Size	A3	Document Number	H55MXV
Date:	Wednesday, April 21, 2010	Sheet	10 of 50



FOXCONN PCEG

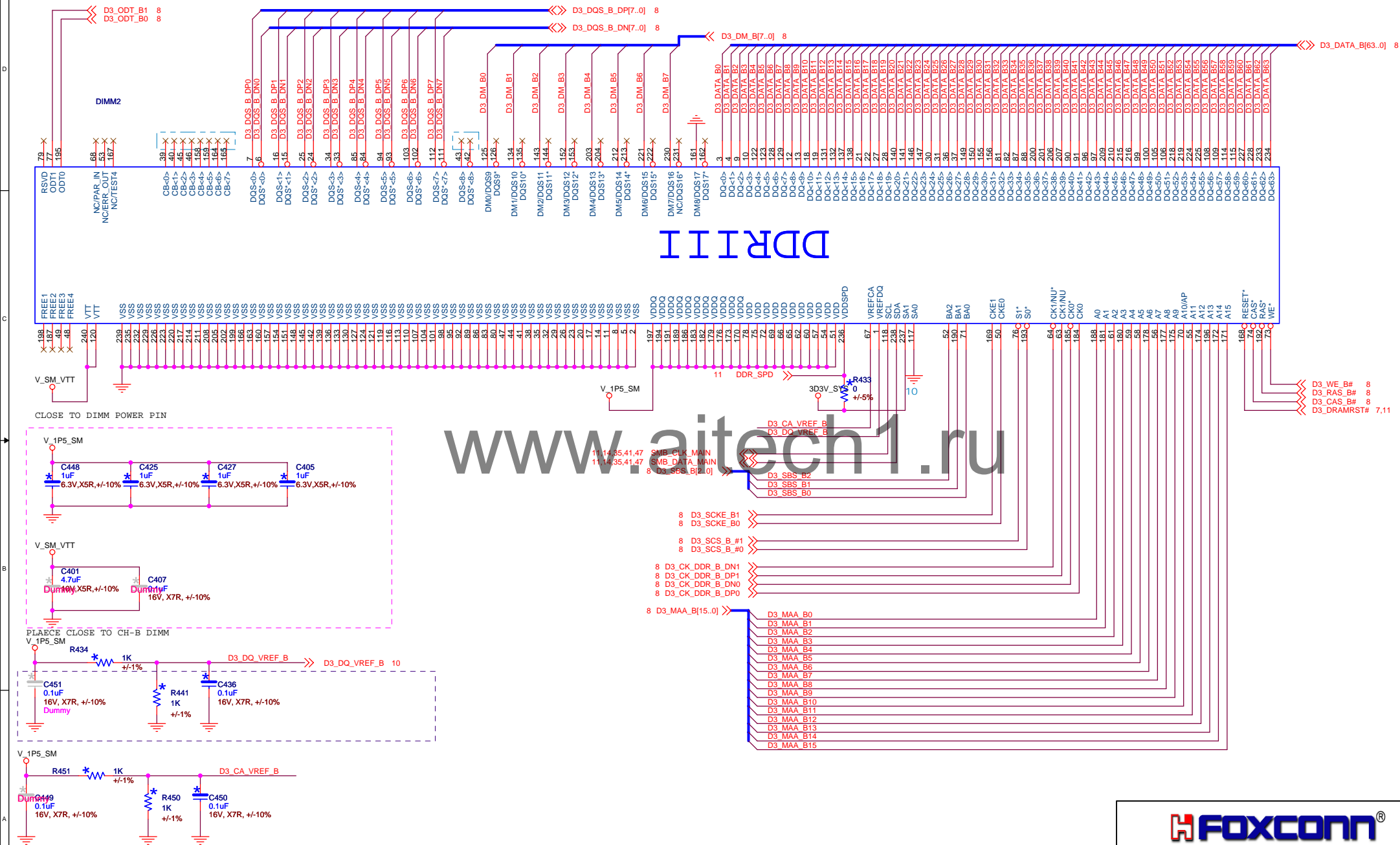
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Size A3	Document Number H55MXV
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Rev	B00
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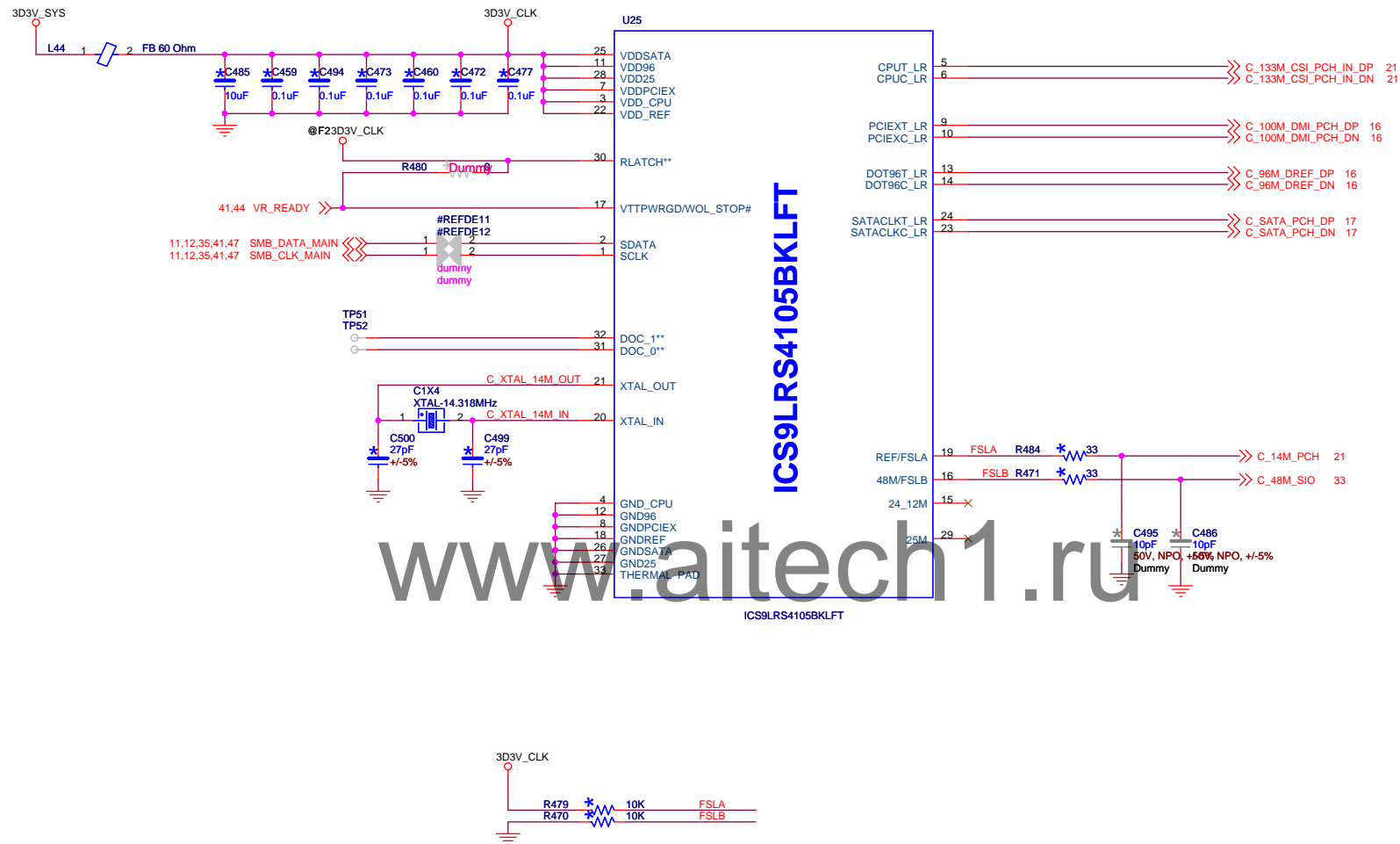
Date: Wednesday, April 21, 2010 Sheet 11 of 50

CHANNEL B BANK 1
SMB ADDRESS:010



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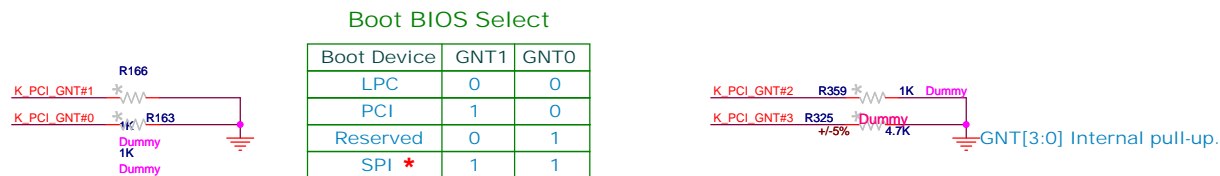
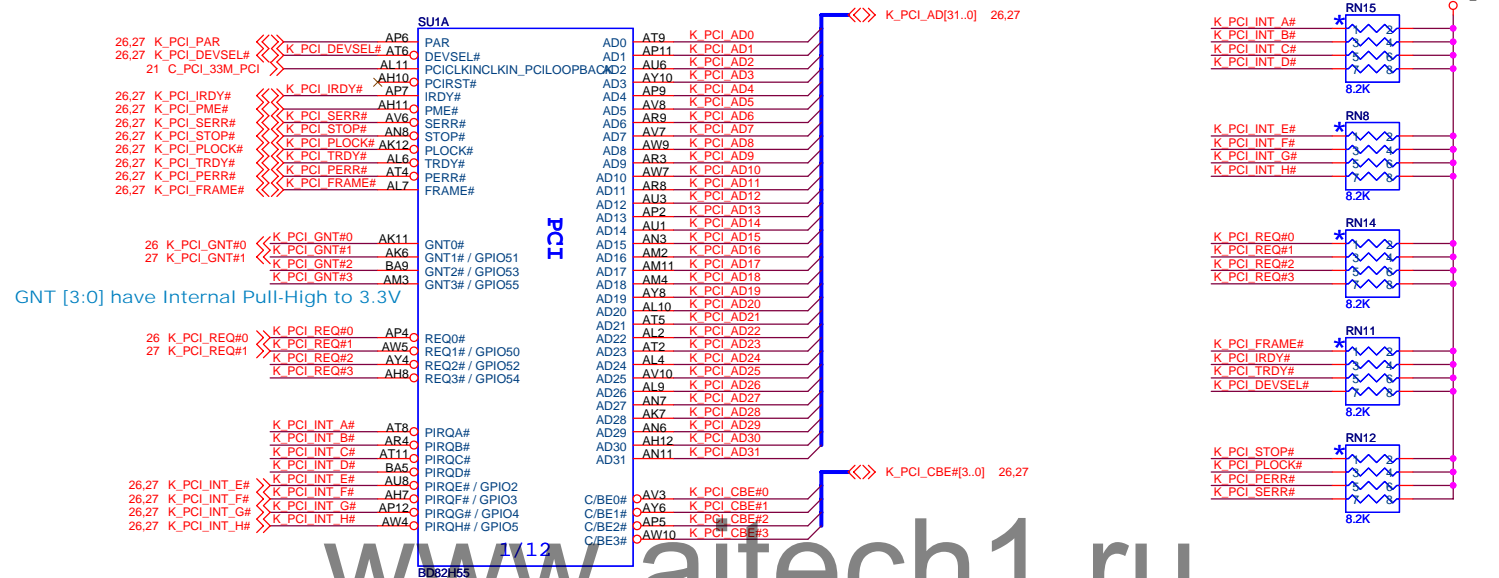
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DDR3 CONN:CHB_1			
Size	Document Number	Rev	
A3	H55MXV	B00	
Date:	Wednesday, April 21, 2010	Sheet	12 of 50



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FOXCONN PCEG

Title		CLOCK GEN
Size	Document Number	H55MXV
A3		
Date:	Wednesday, April 21, 2010	Sheet 14 of 50
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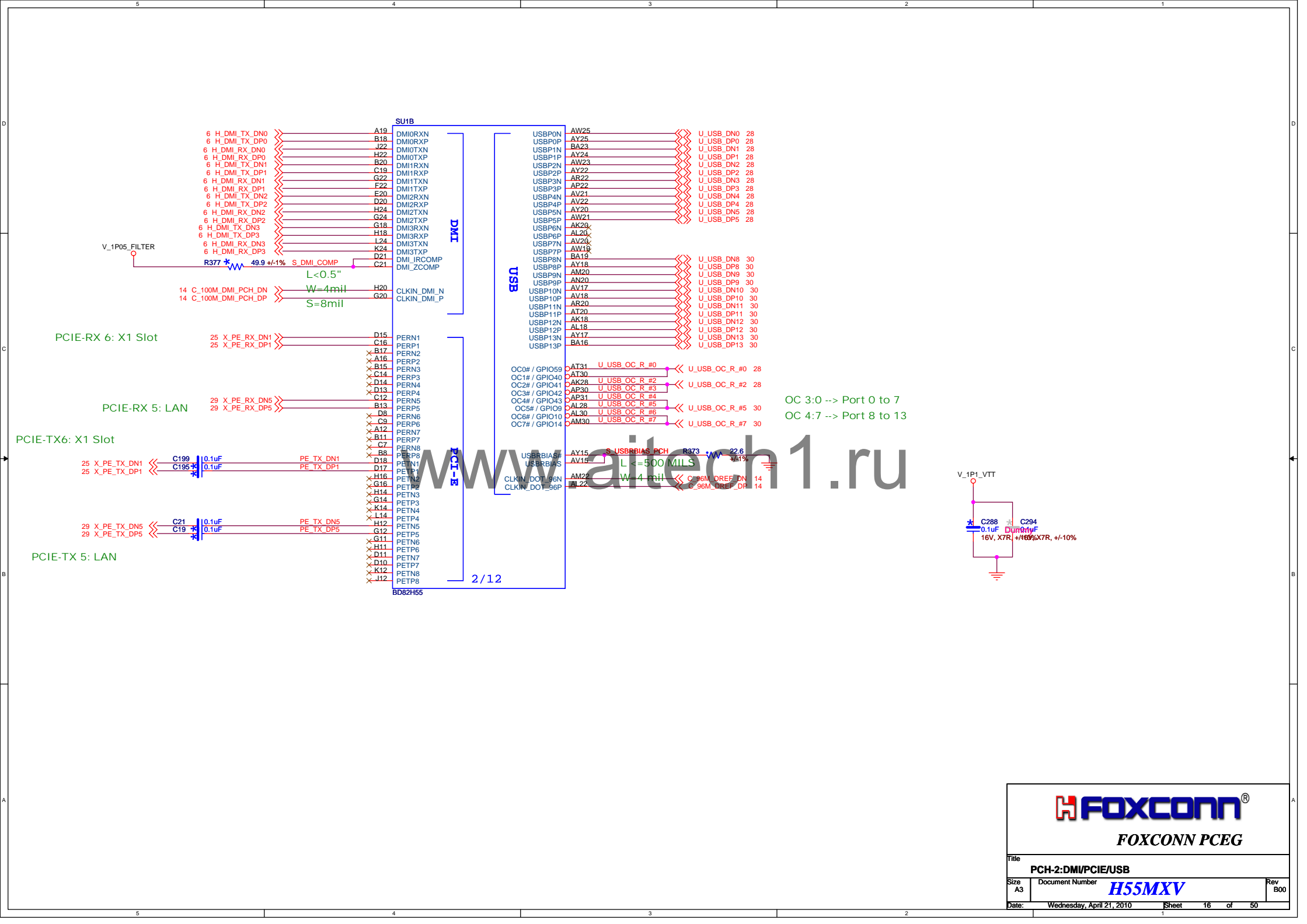
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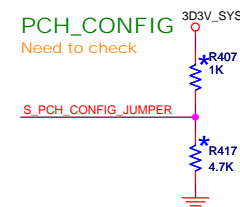
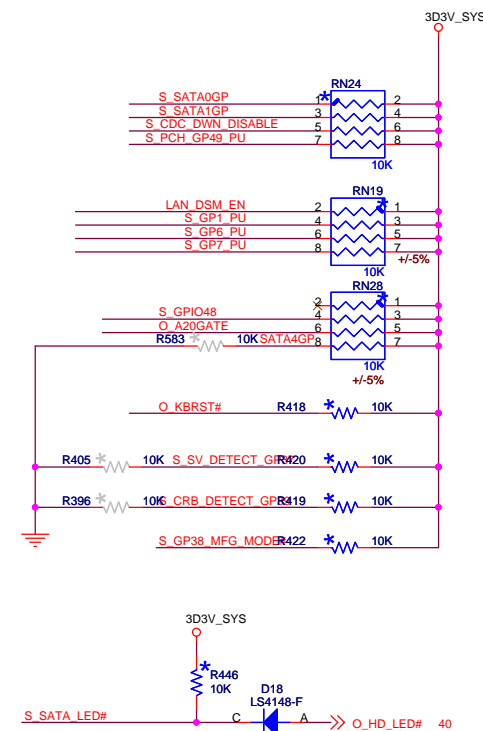
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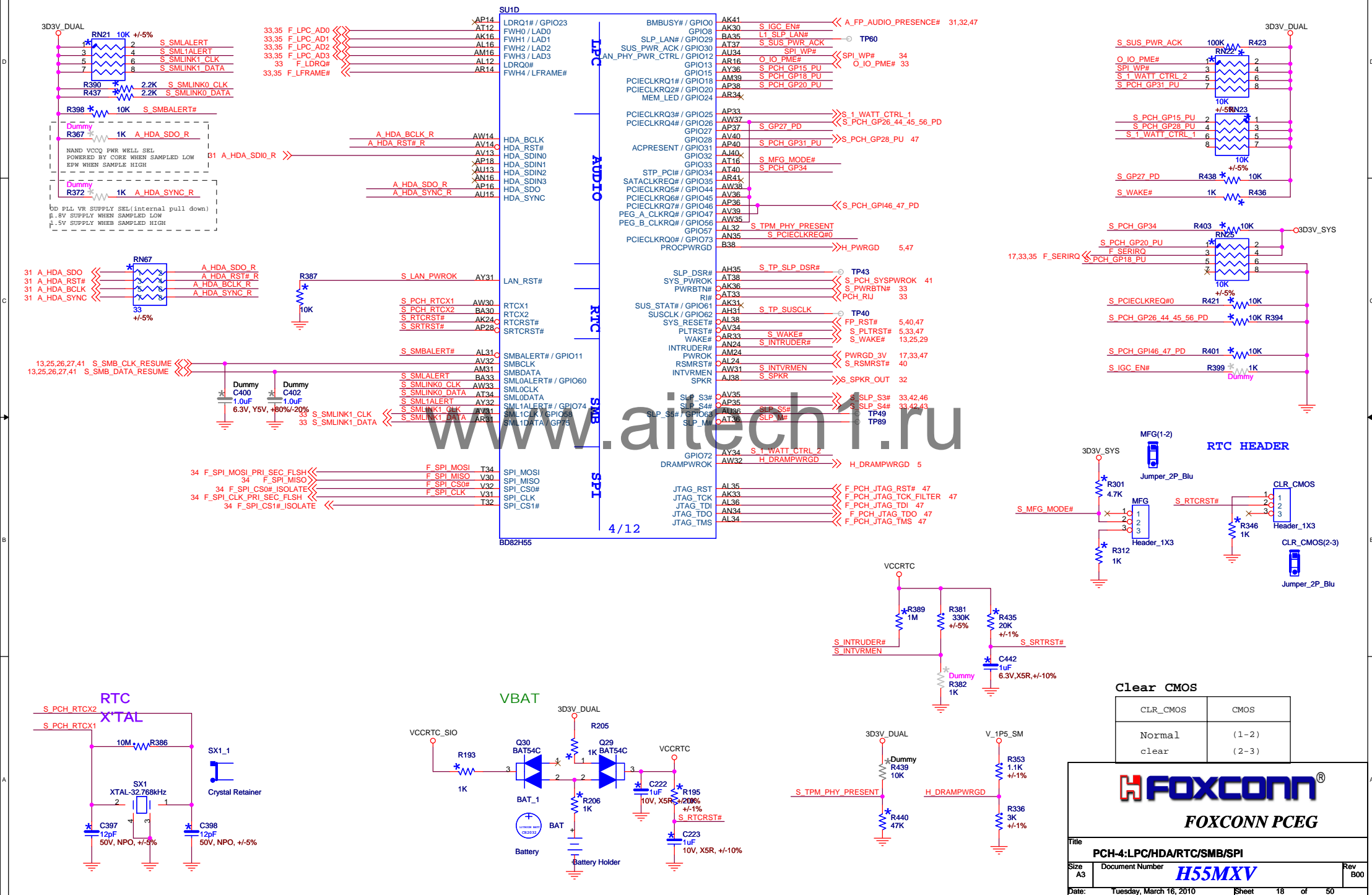
Size A3 Document Number **H55MXV**

Date: Wednesday, April 21, 2010 Sheet 15 of 50 Rev 500





BOARD ID TABLE		
GP37	GP39	BOARD STYLE
1	1	6K
1	0	8K

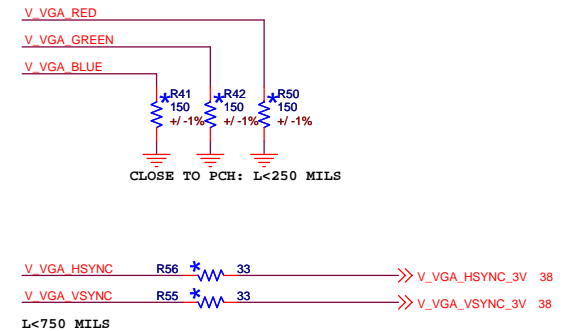
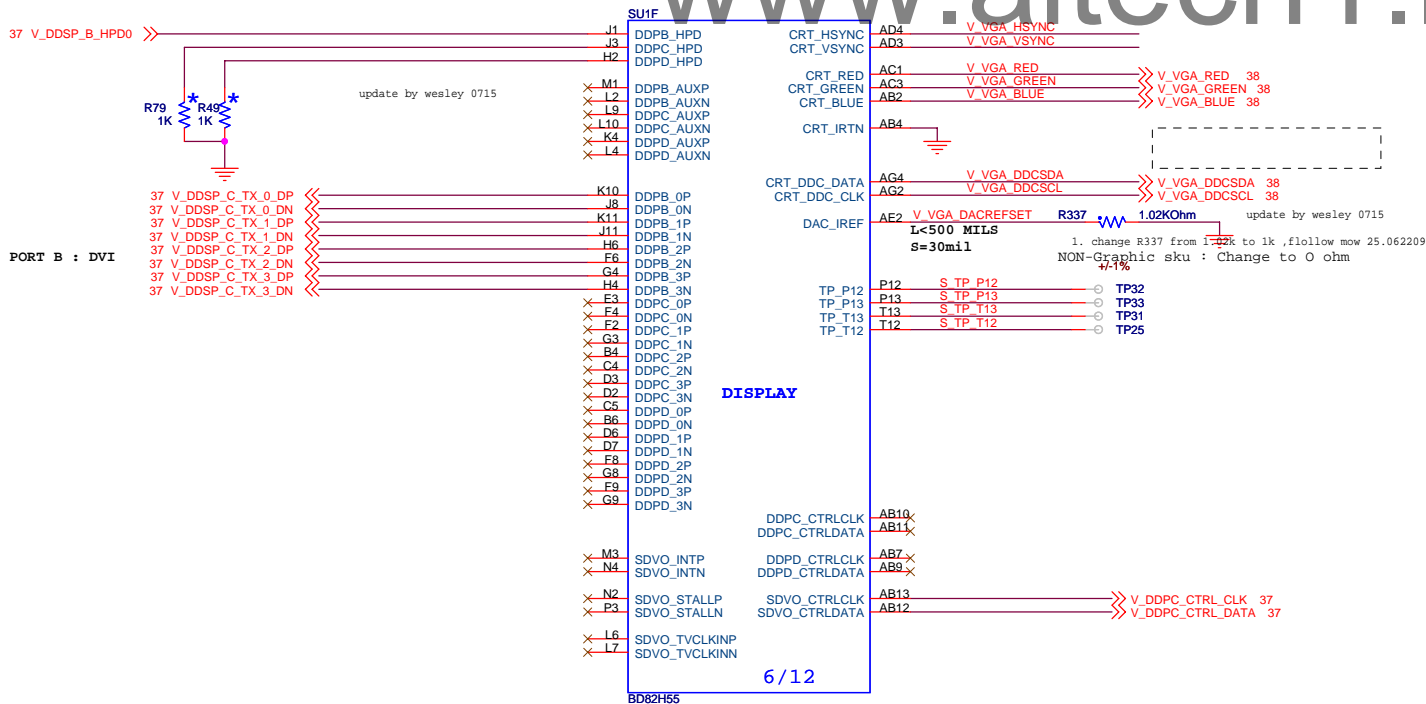
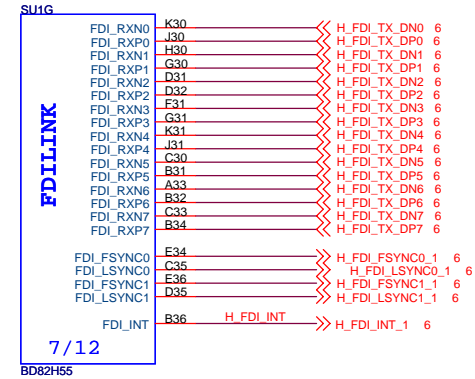
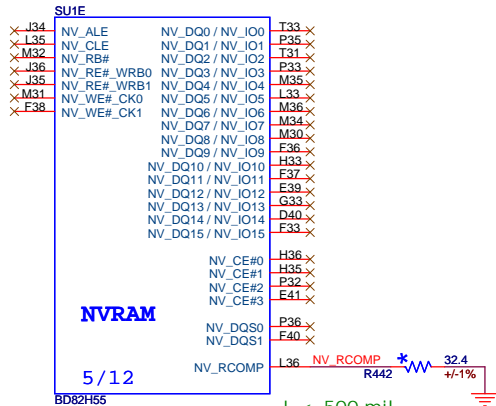


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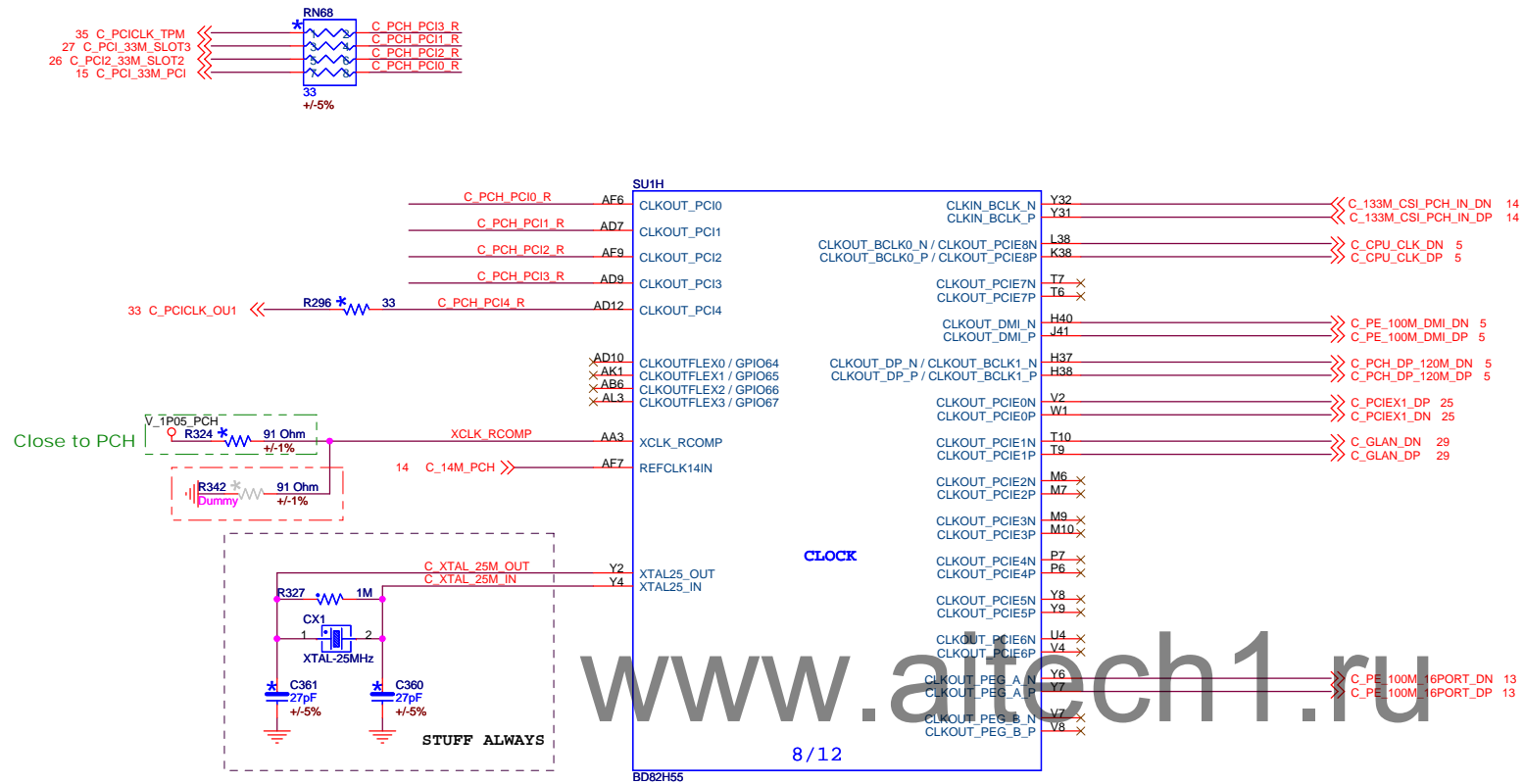
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Size	Document Number		Rev		
A3	H55MXV		500		
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FOXCONN PCEG

Title		PCH-7:DISPLAY	
Size	A3	Document Number	H55MXV
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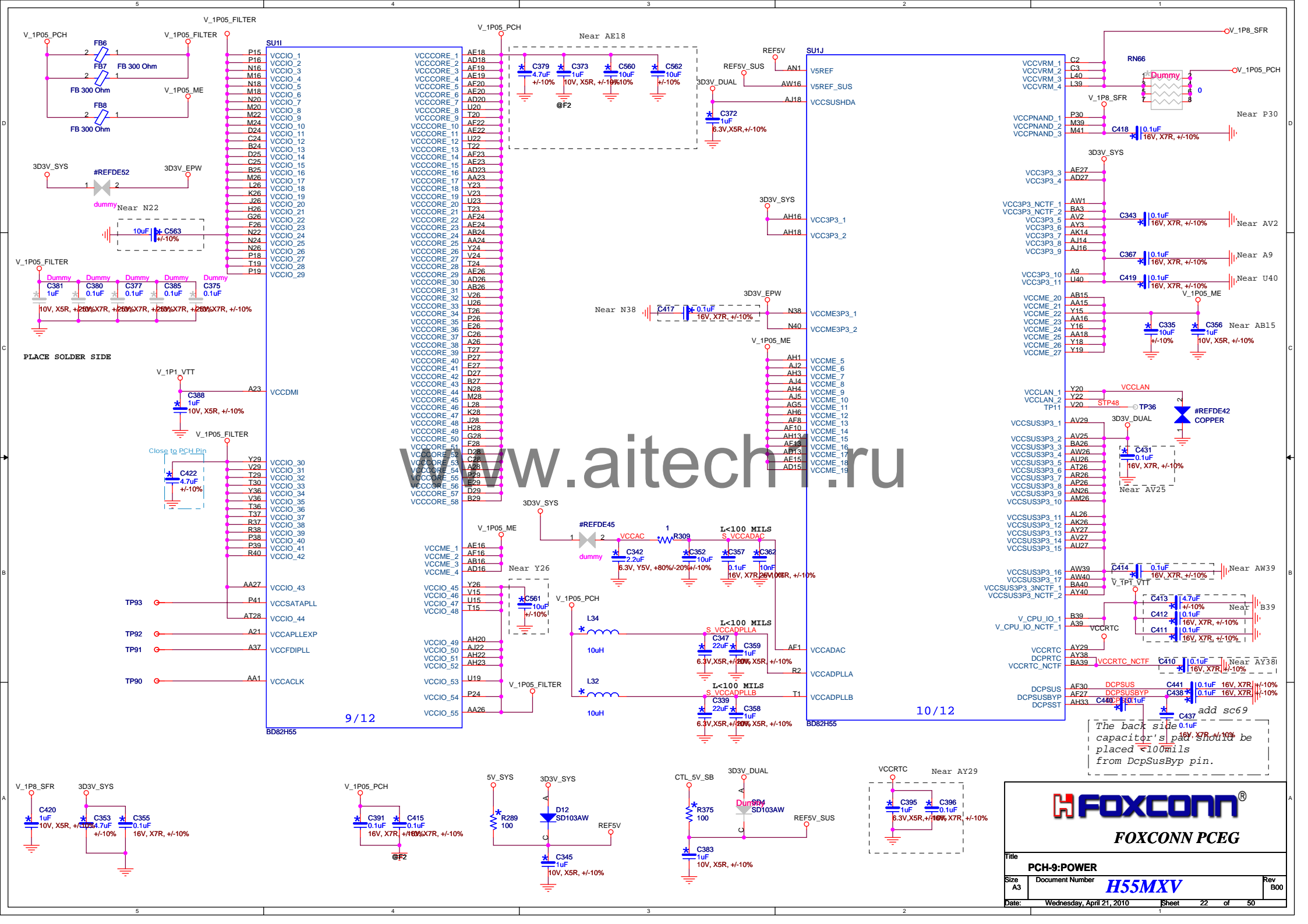


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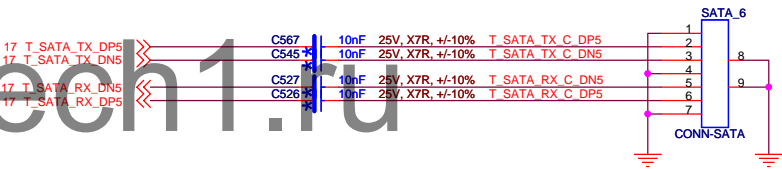
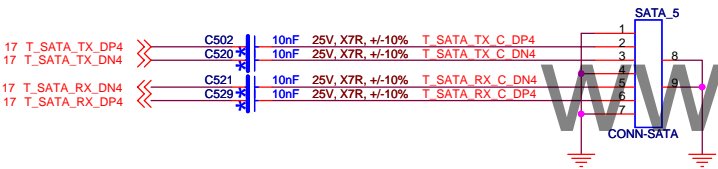
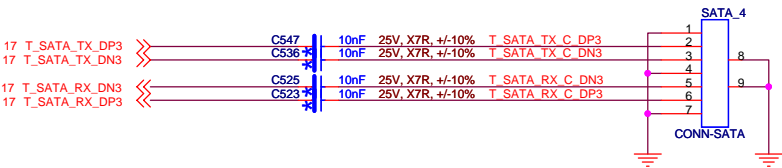
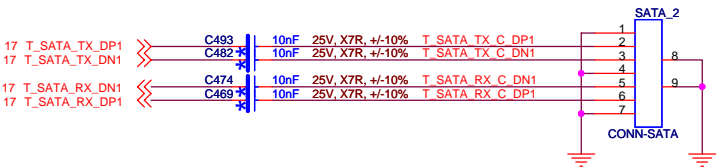
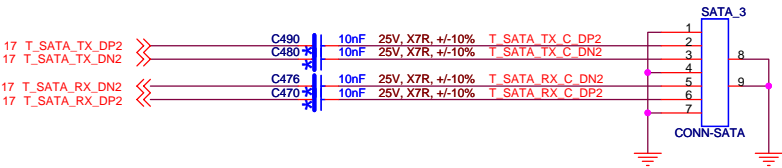
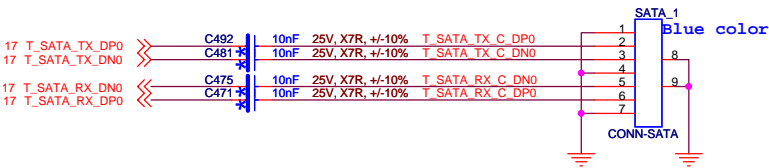


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Size	Document Number	H55MXV
A3		
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		Rev 500



SATA x 6



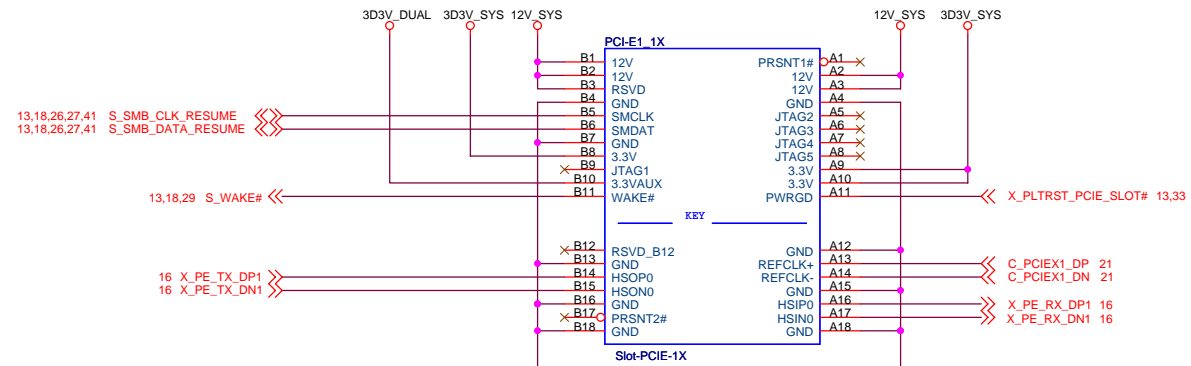
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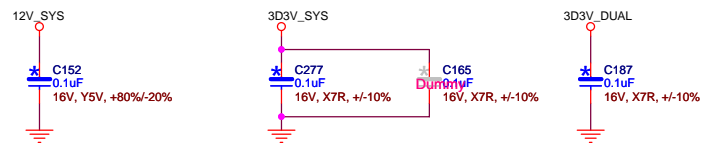
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SATAx4/ESATA Buffer			
Size	Document Number	Rev	
A3	H55MXV	500	
Date:	Wednesday, April 21, 2010	Sheet	24 of 50

PCIE X1 SLOT

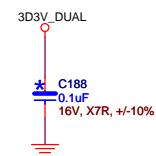
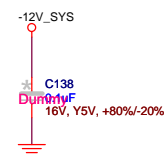
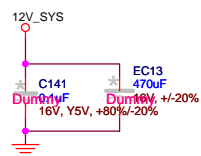
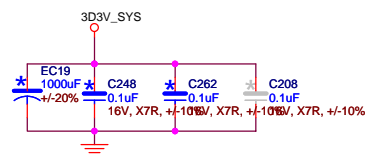
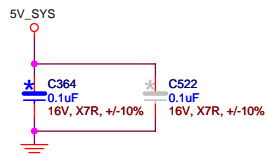
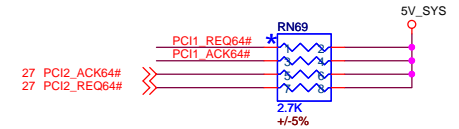
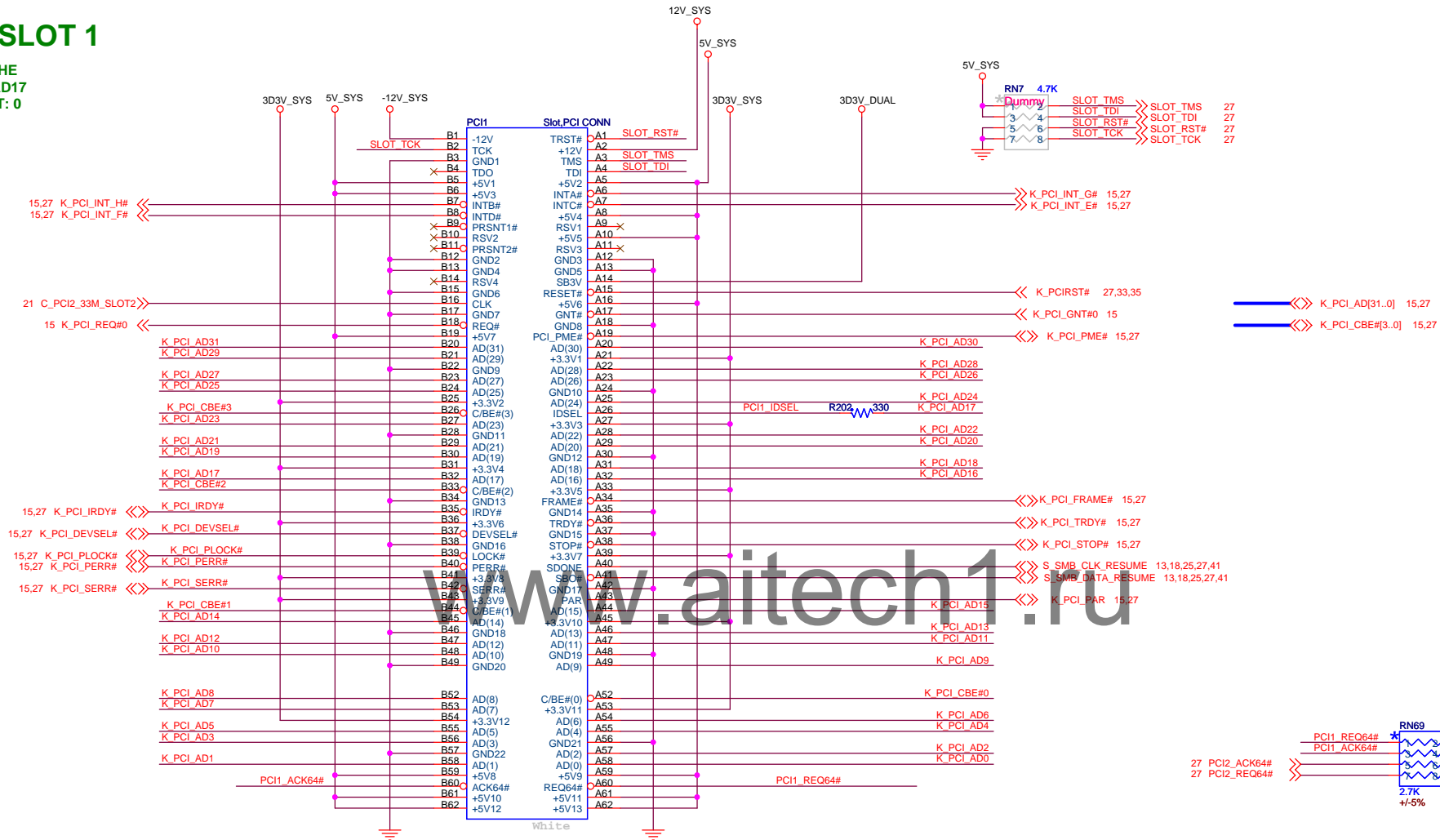


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PCI SLOT 1

IRQ: FGHE
IDSEL: AD17
REQ/GNT: 0

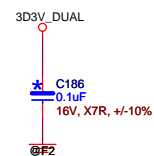
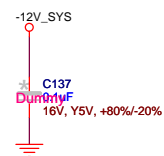
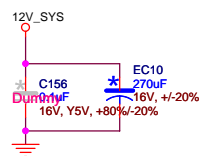
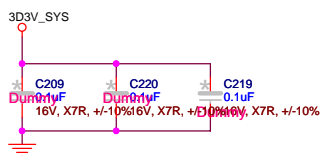
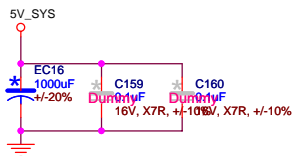
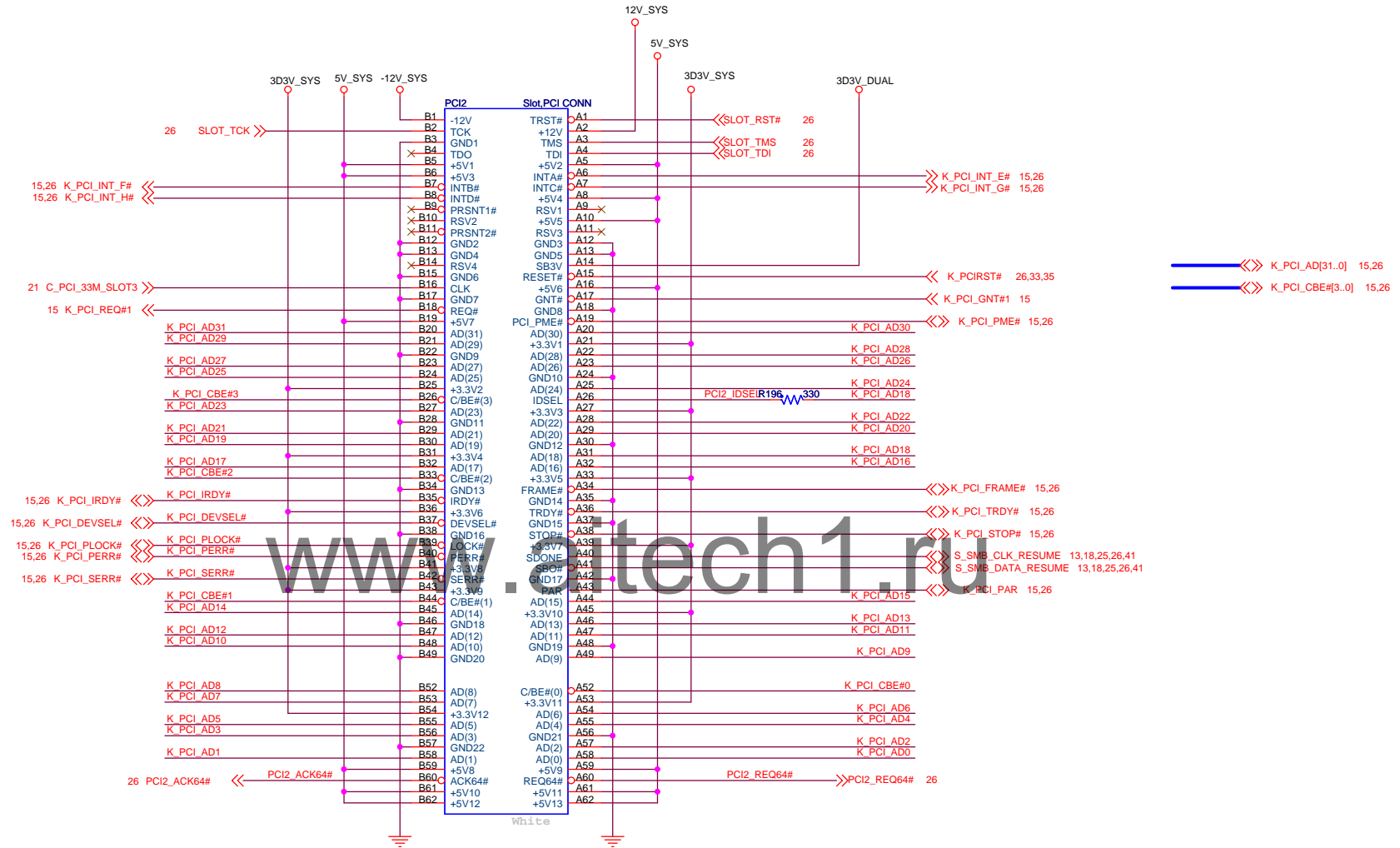


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Title			PCI SLOT 1
Size	Document Number	H55MXV	
A3			Rev 500
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PCI SLOT 2

IRQ: GFEH
IDSEL: AD18
REQ/GNT: 1

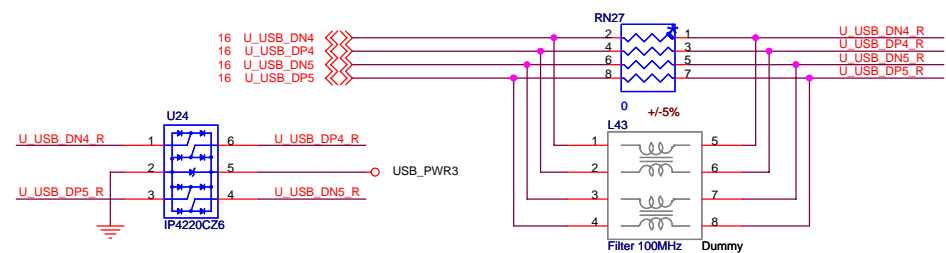
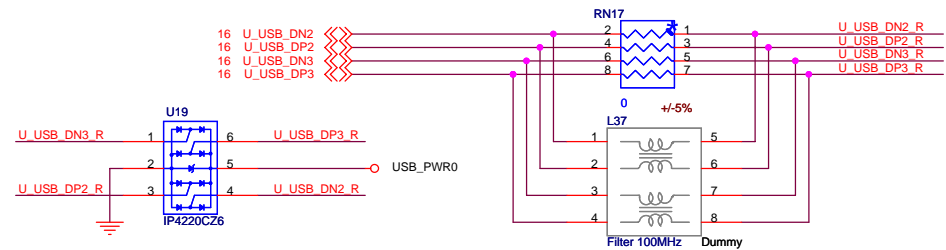
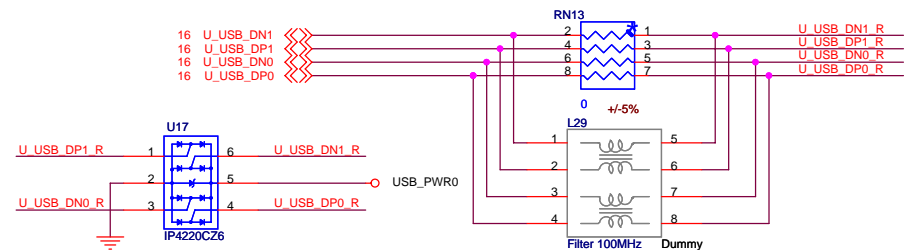
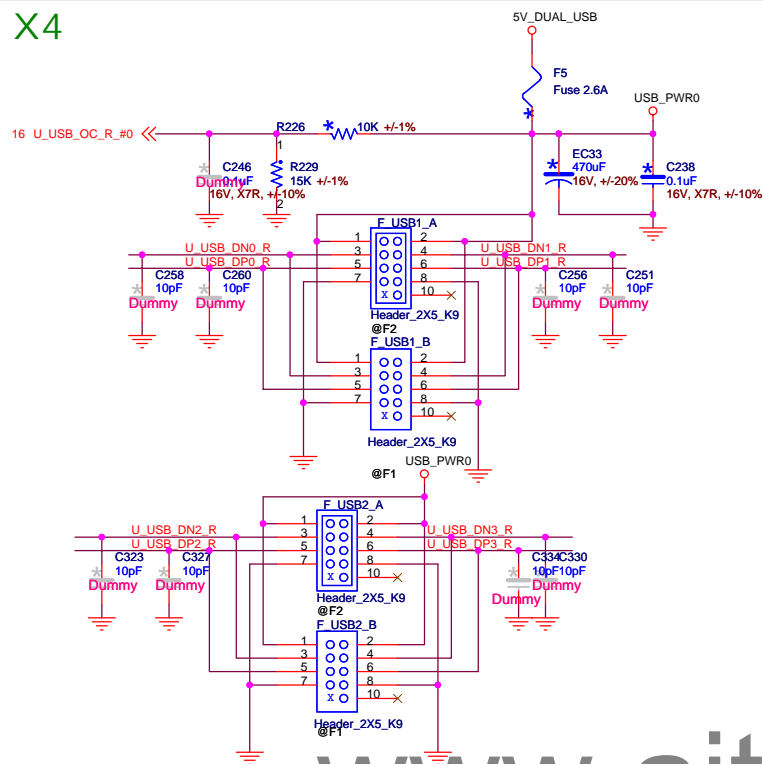


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Title			PCI SLOT 2
Size	Document Number	H55MXV	
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Front USB Header X4

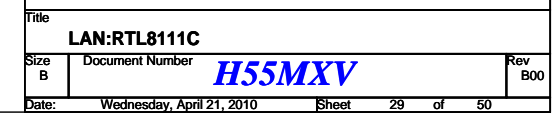
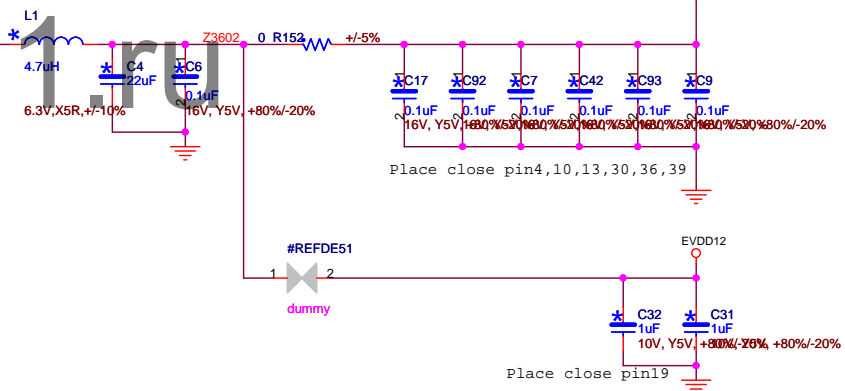
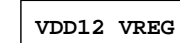
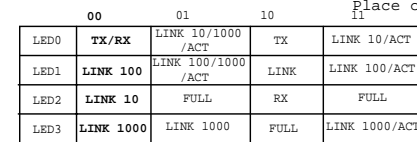
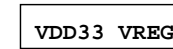
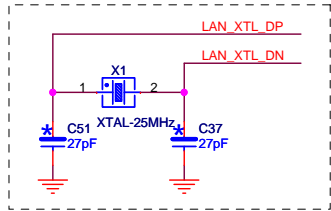


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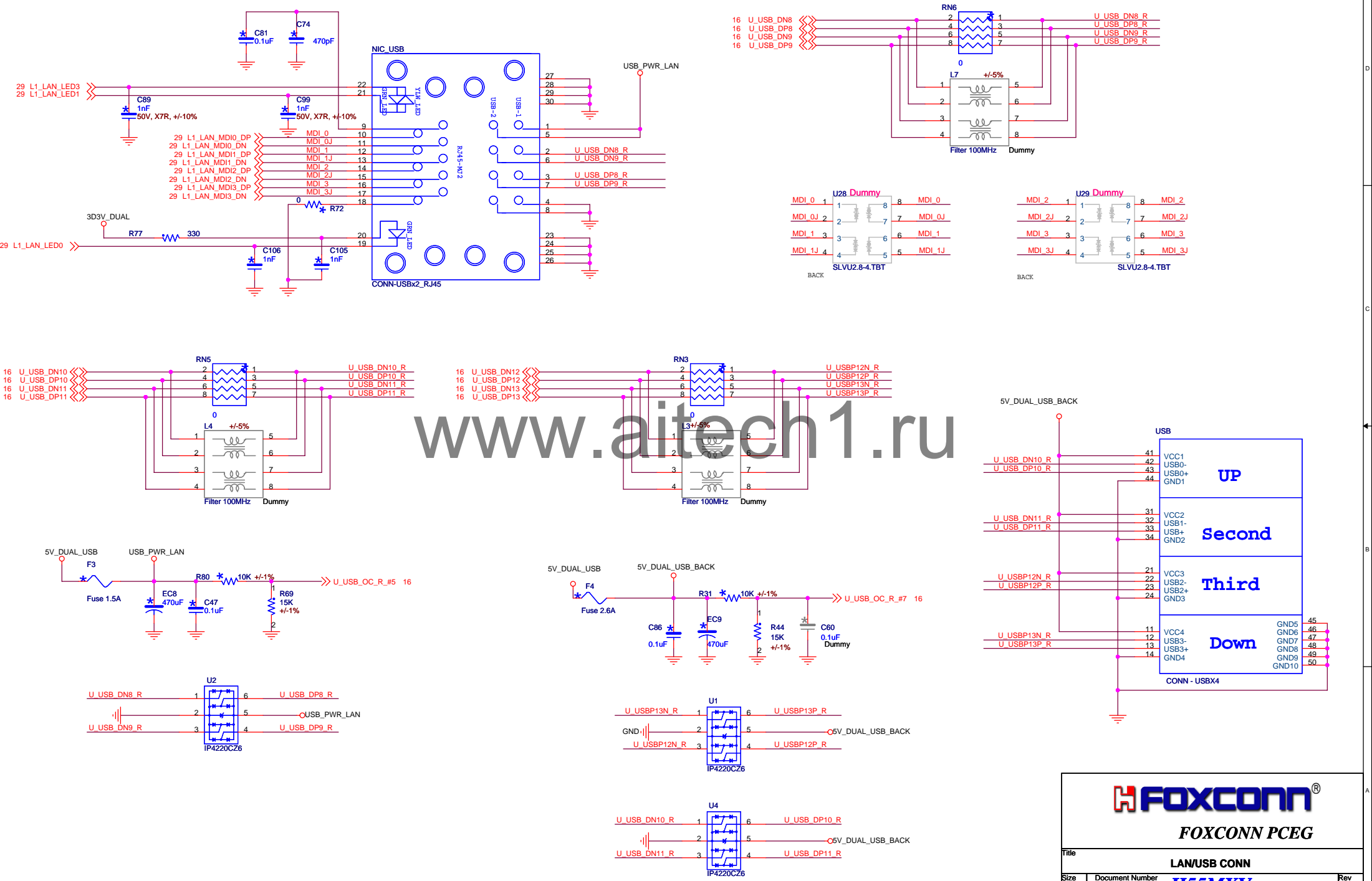
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FOXCONN PCEG

Title			Front USB Header
Size	Document Number	H55MXV	
A3			Rev 500
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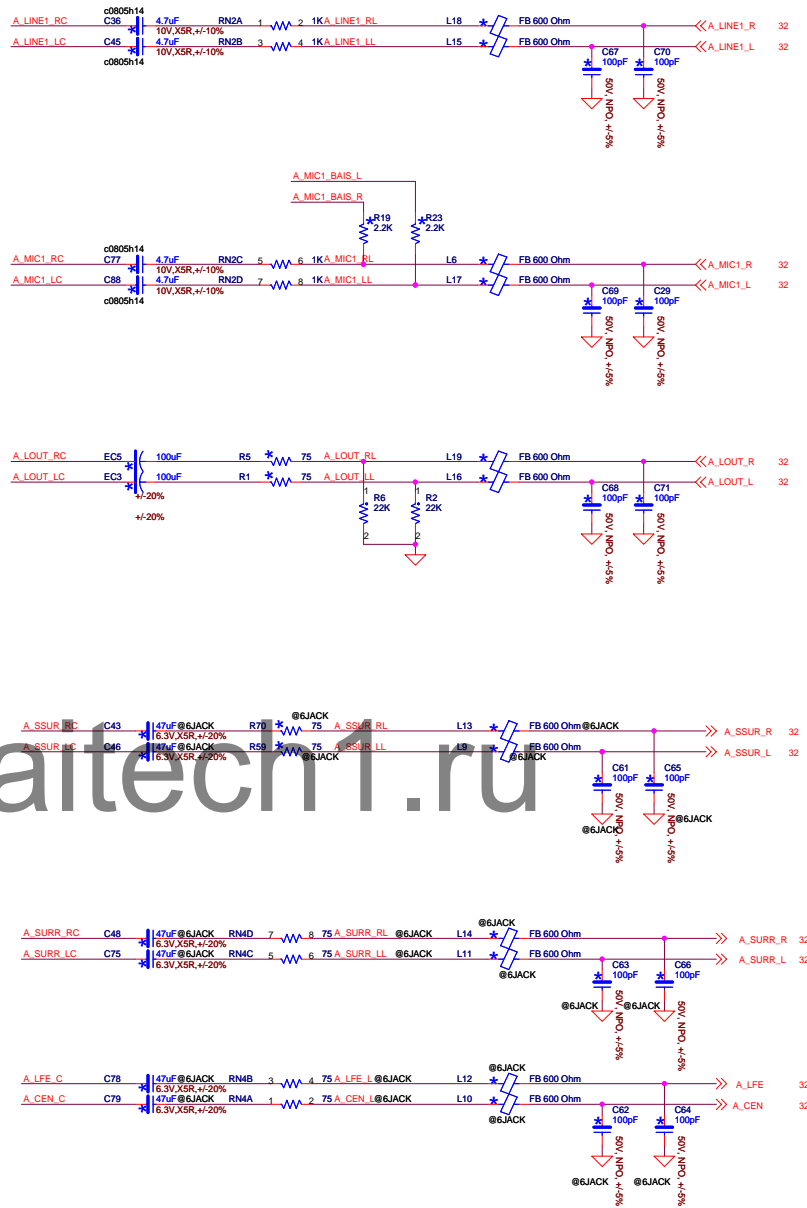
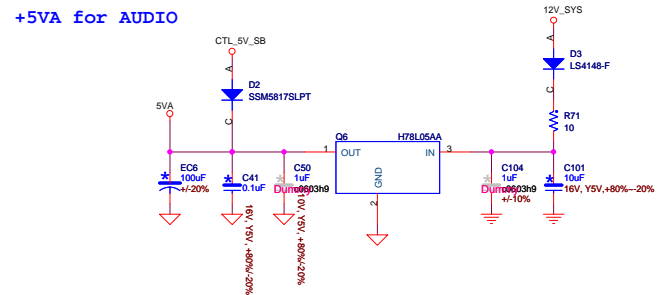
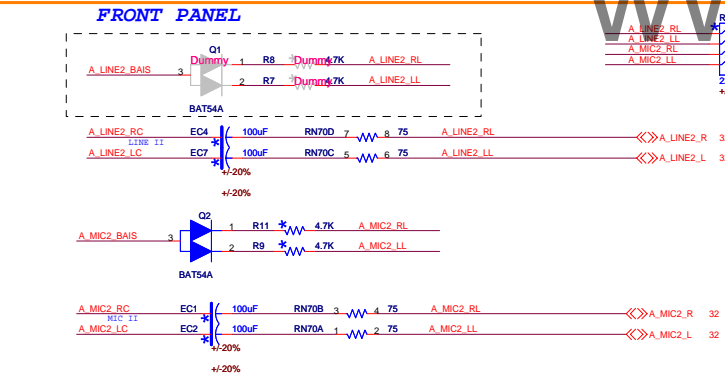
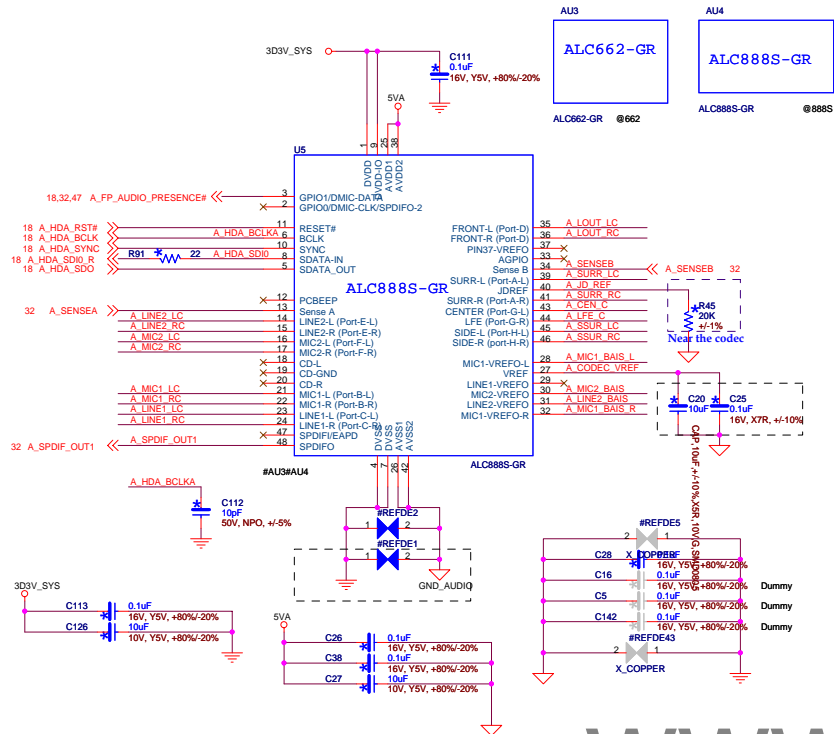
LAN/USB CONNECTOR



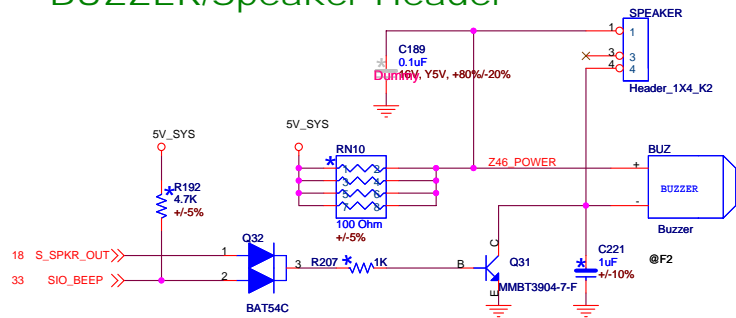
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FOXCONN PCEG

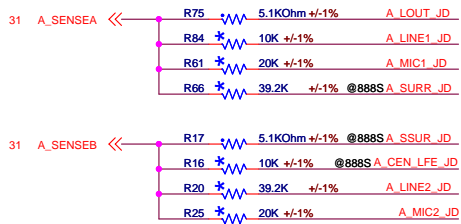
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Size	Document Number	H55MXV			Rev
A3				500	
Date:	Wednesday, April 21, 2010			Sheet	30 of 50



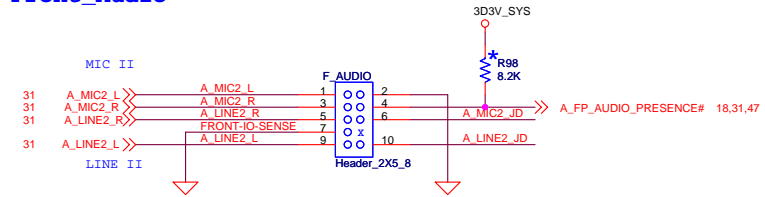
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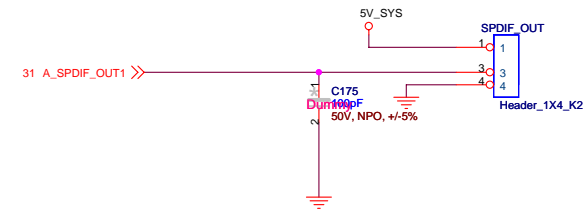
JACK SENSE



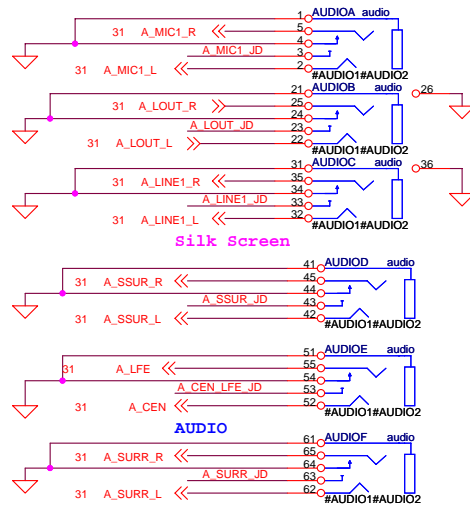
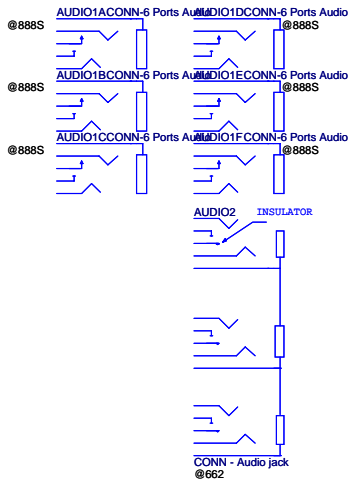
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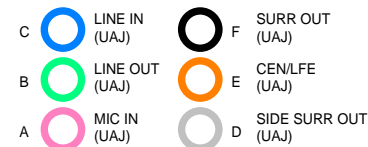
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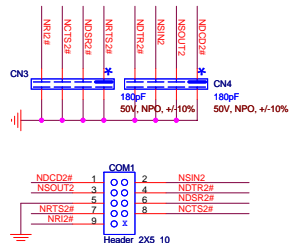
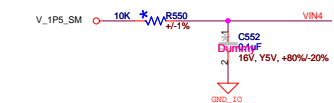
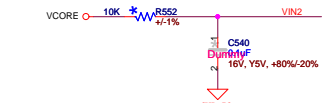
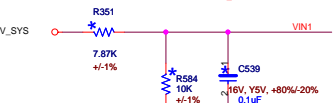
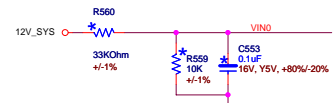
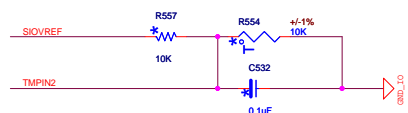


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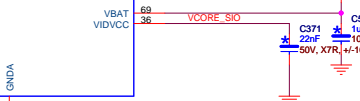
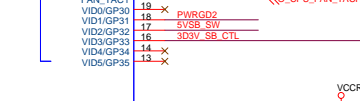
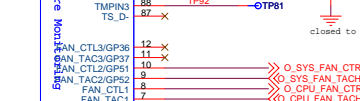
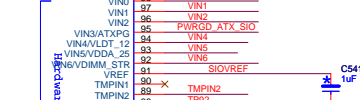
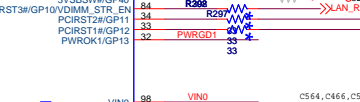
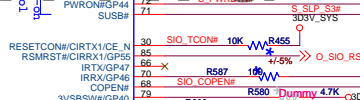
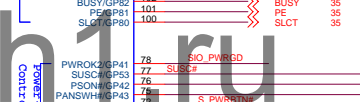
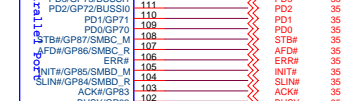
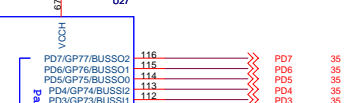
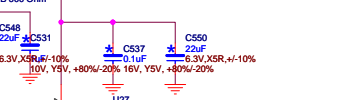
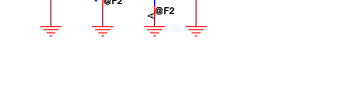
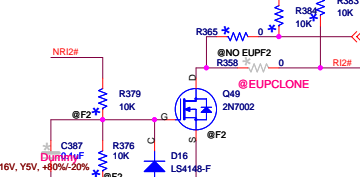
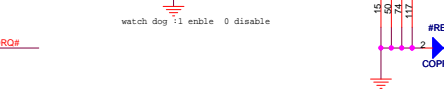
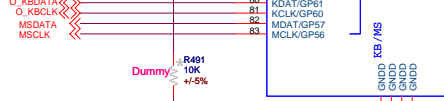
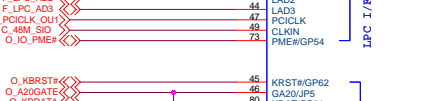
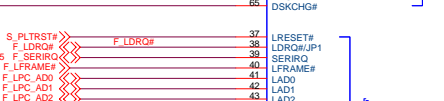
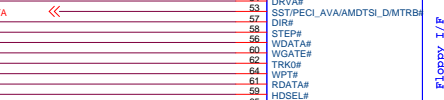
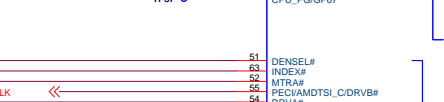
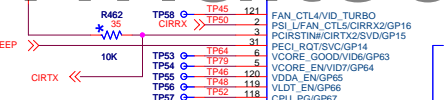
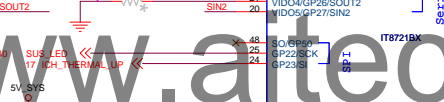
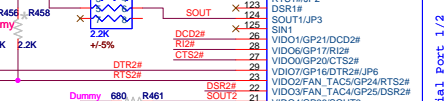
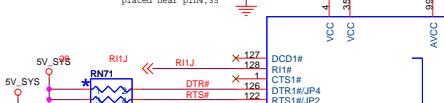
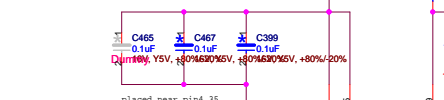
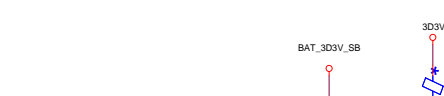
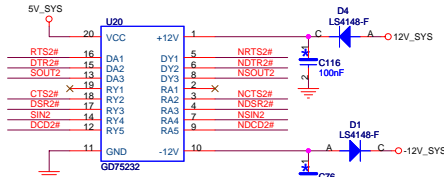
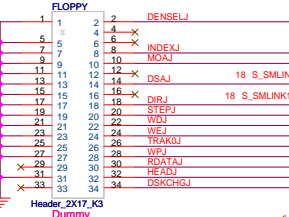
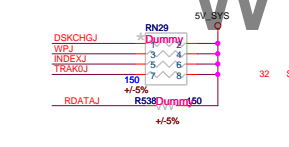
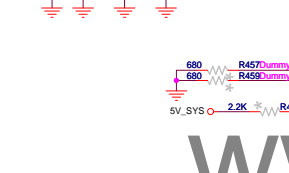
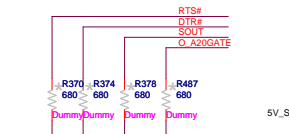


Audio Jack

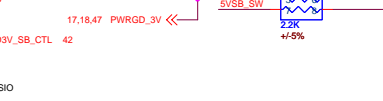
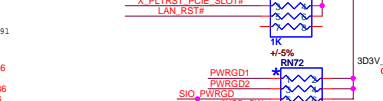
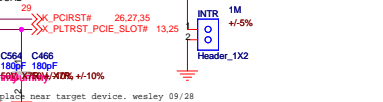
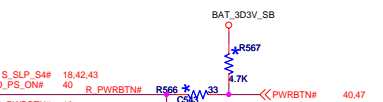
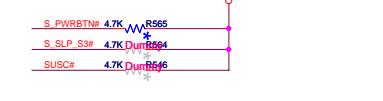
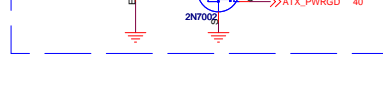
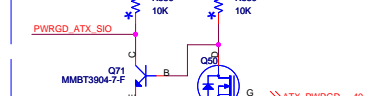
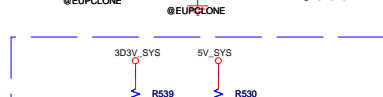
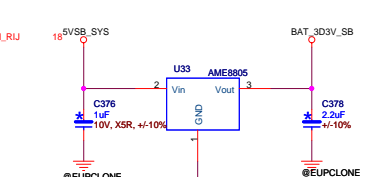




COM2 HEADER



BAT_3D3V_SB



IT8721BX Power On Strapping Options

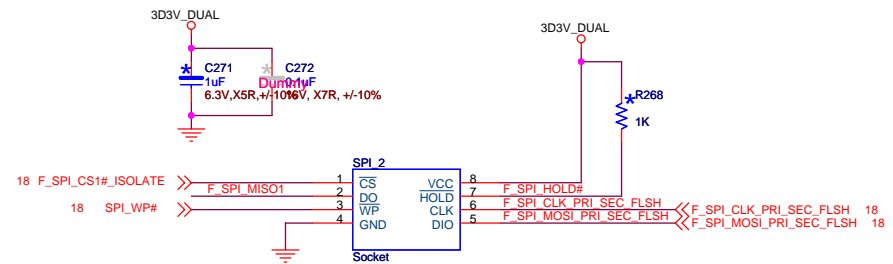
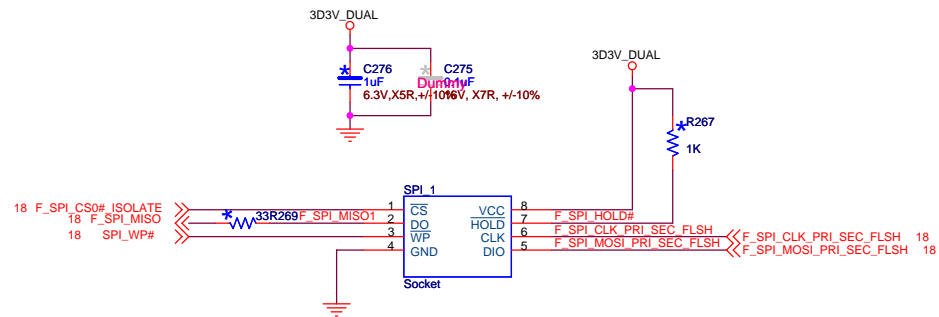
Symbol	value	Description
JP3	Flashseg1_EN	1 Disabled.
Pin 124	0	Flash I/F Address Segment 1 is enabled
JP4	K8PWR_EN	1 K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	10 The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
Pin 124 & 46	01	The default value of EC Index 15h/16h/17h is 7fh(Fan off)
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin 46	0	Enable WDT to rest PWROK
JP2 & JP6	VIDO_SEL	11 Disable VID/SVID output pins
Pin 122 & 29	10	For AMD platform(serial)
	01	For Intel platform
	00	For AMD platform(parallel)

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SPI




SPI_ROM1



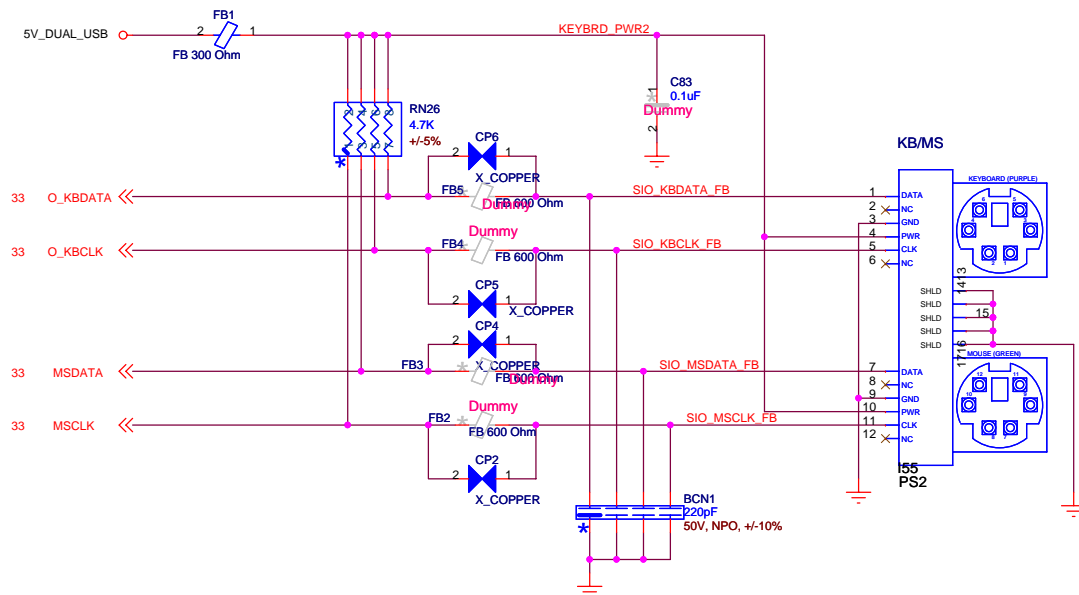
MX25L3205DPI-12G

SPI_ROM2



MX25L3205DPI-12G

PS2 KB / MS



FOXCONN PCEG

Title

SPI/KBUSB

Size
A2

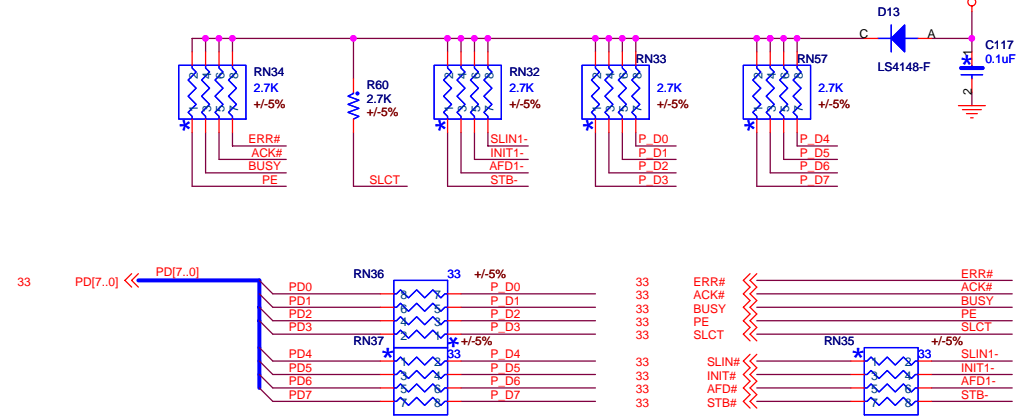
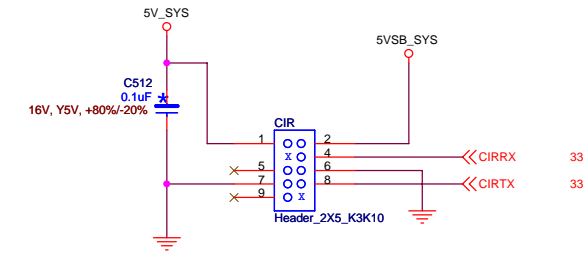
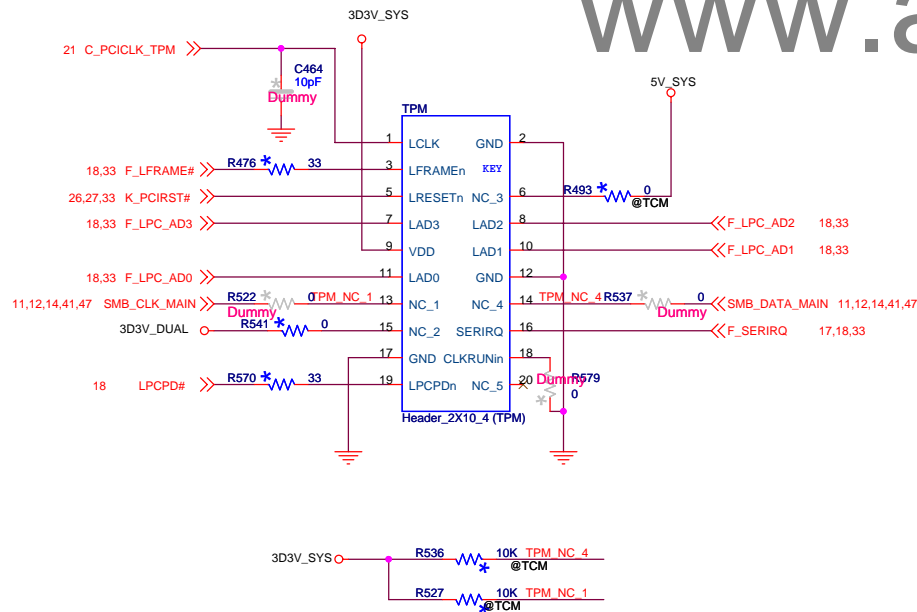
Document Number

H55MXVRev
B00

Date: Wednesday, April 21, 2010

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TPM/TCM Connector



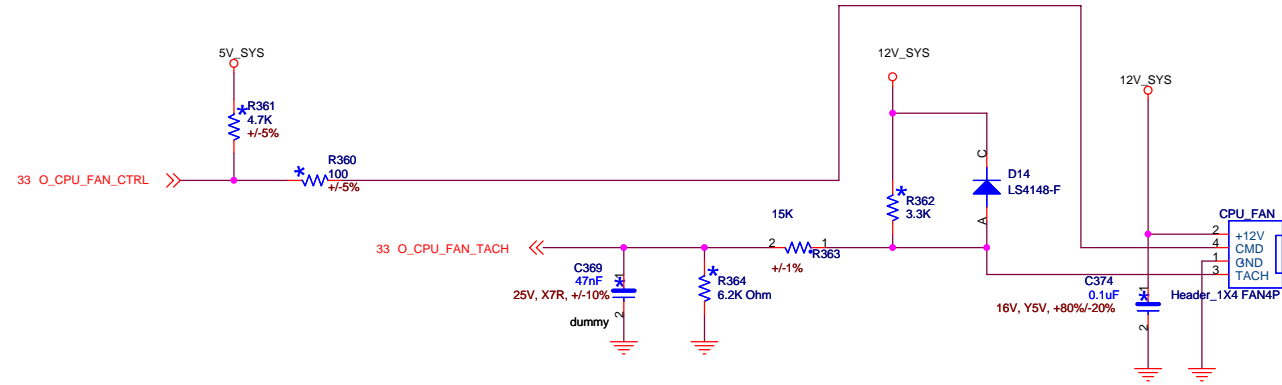
LPT PORT

FOXCONN

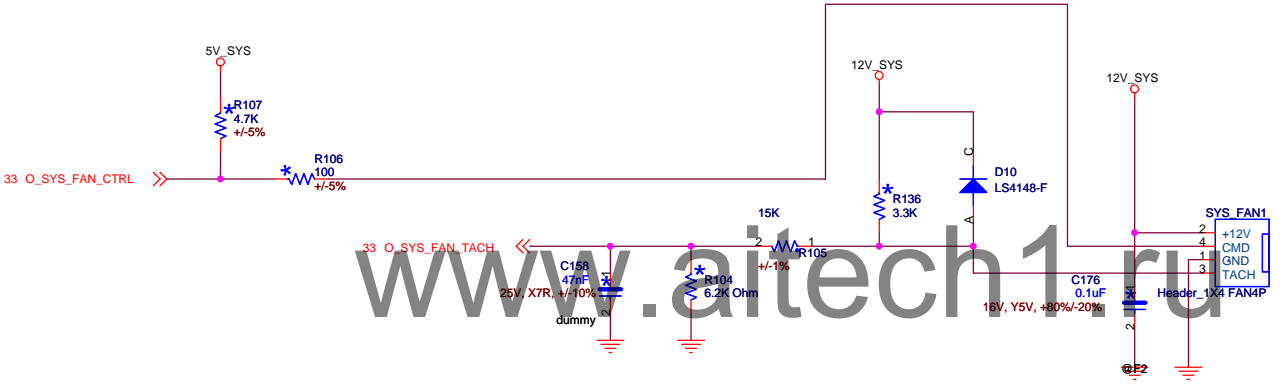
FOXCONN PCEG

Title		PCI SLOT
Size	Document Number	H55MXV
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CPU FAN



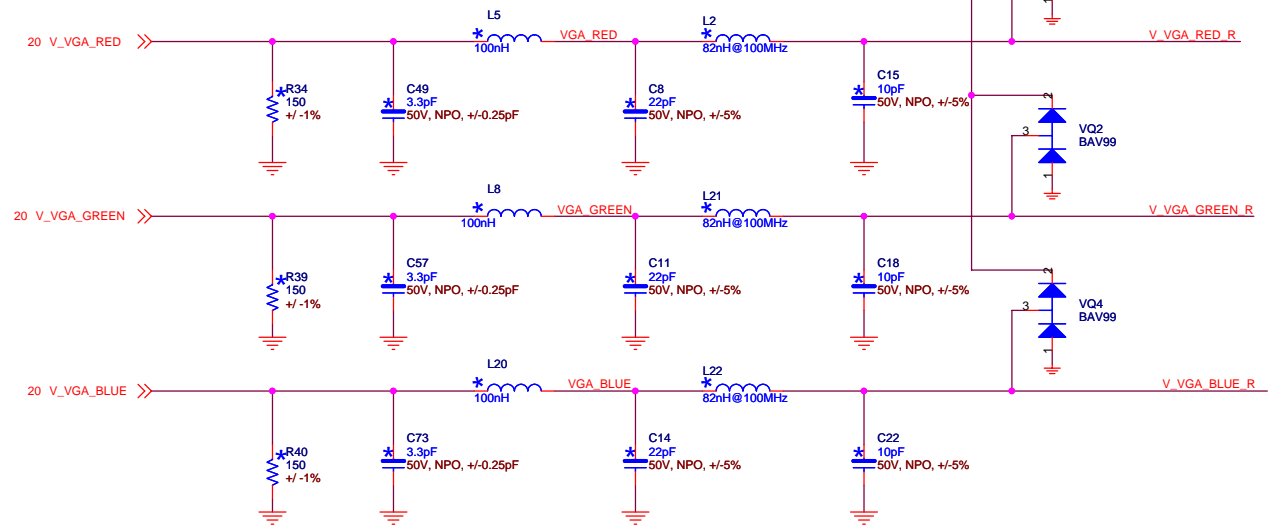
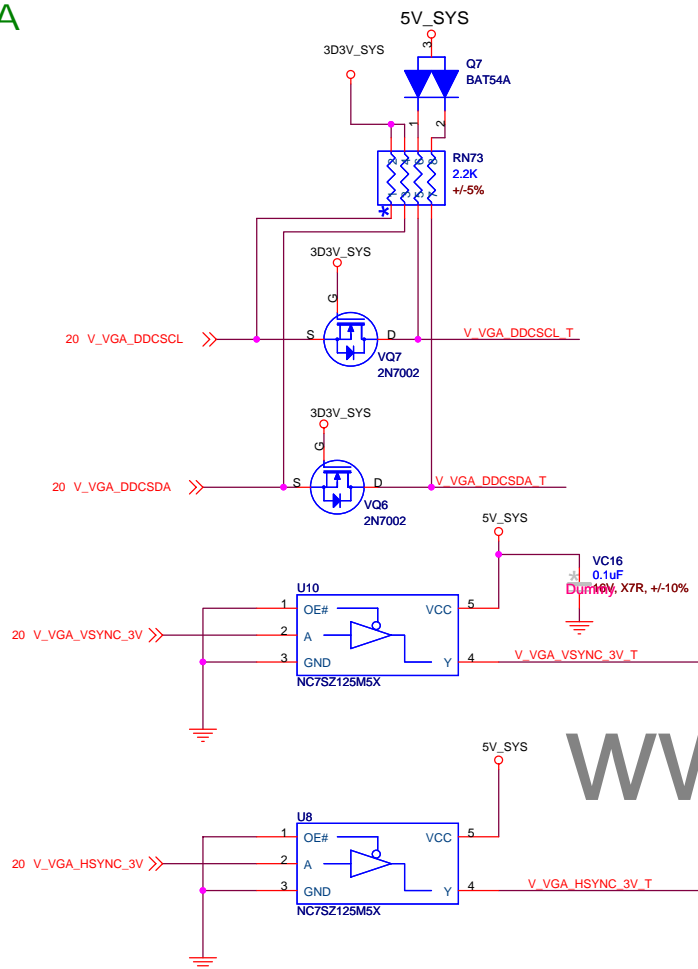
SYSTEM FAN



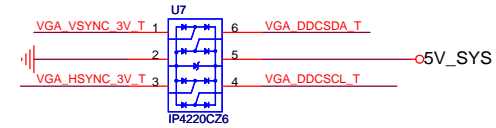
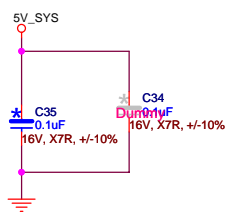
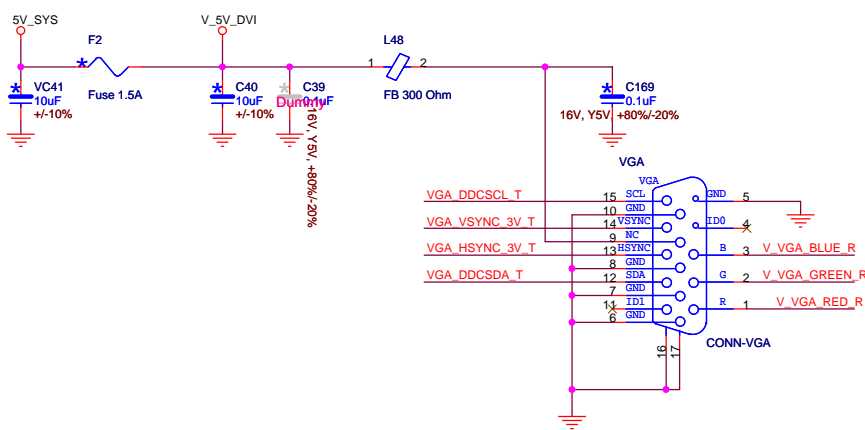
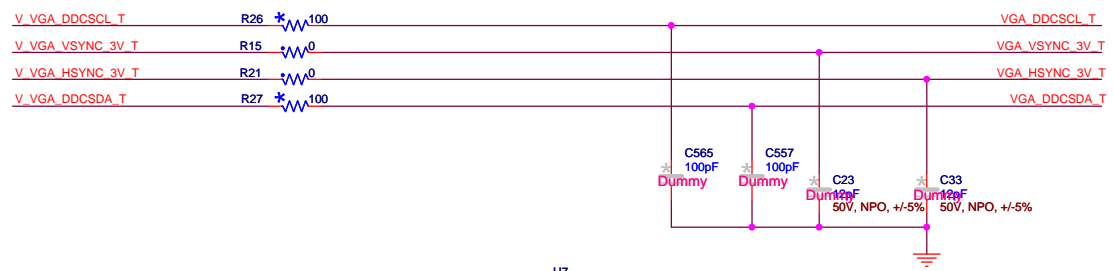
FOXCONN PCEG

Title			
CPU & System FAN			
Size	Document Number	Rev	
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VGA



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FOXCONN PCEG

Title		DVI-I (Analog)	
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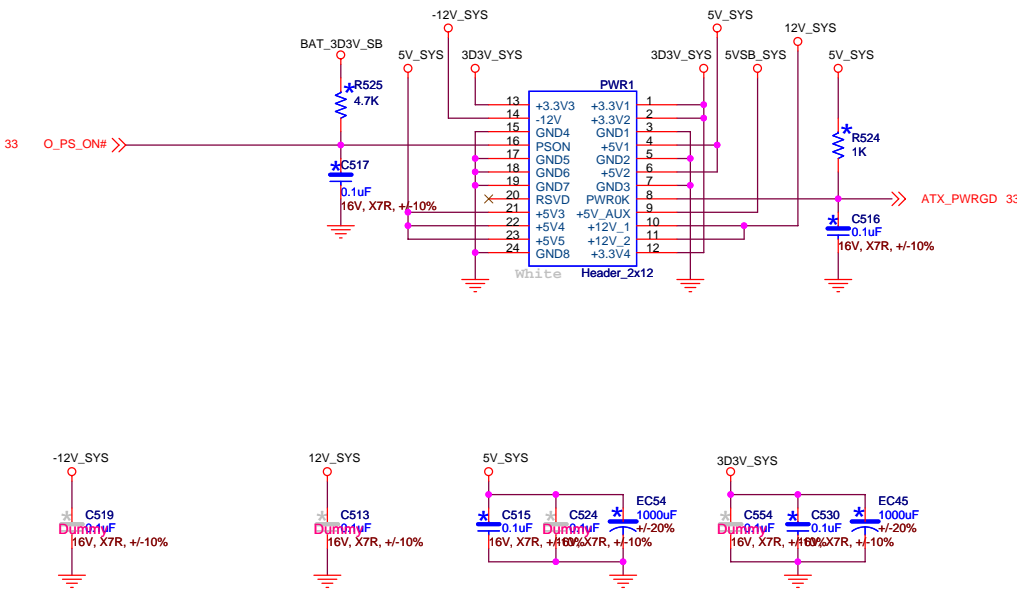
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FOXCONN PCEG

Title			BUZZER		
Size	Document Number		Rev		
A3	H55MXV		500		
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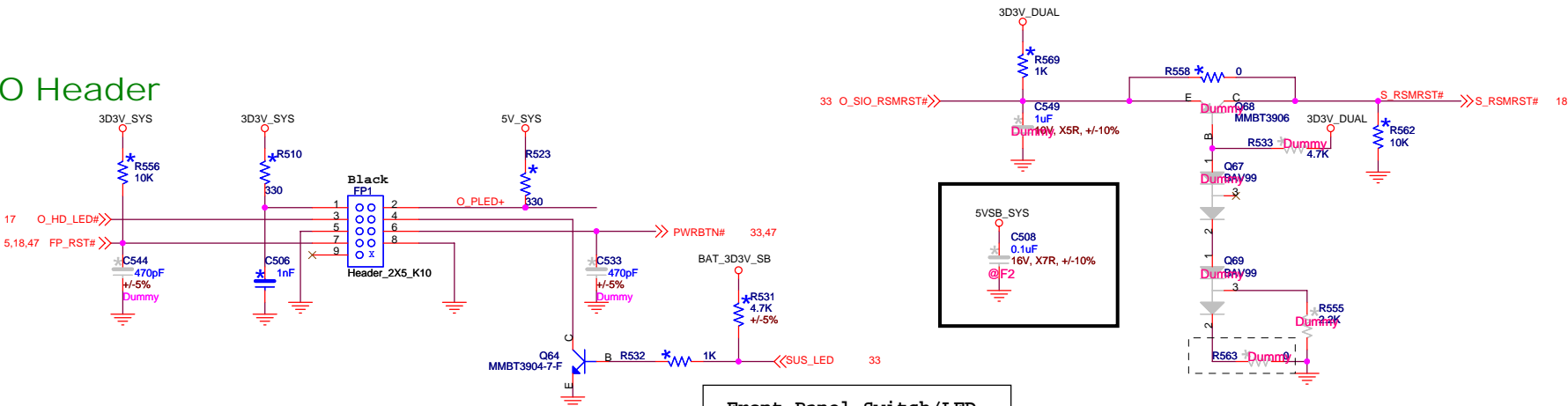
ATX POWER CONNECTOR



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RESUME RESET LOGIC

Front I/O Header



S0 : Power LED is on;
S1 : Power LED is blinking;
S3~S5: Power LED is off.

Front Panel Switch/LED					
HD_LED+	1	2	Power		
HD_LED-	3	4	Power LED(Green)		
GND	5	6	Power button		
Reset button	7	8	Detect pin		
Detect pin	9	10	Key		



FOXCONN PCEG

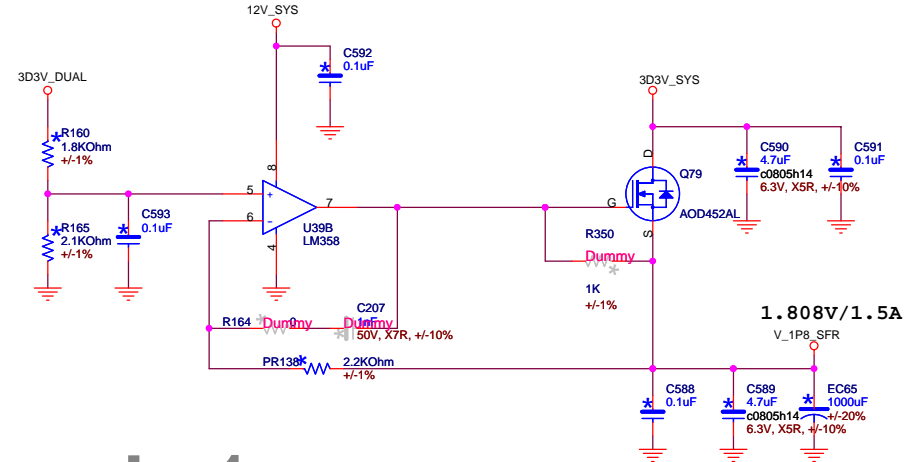
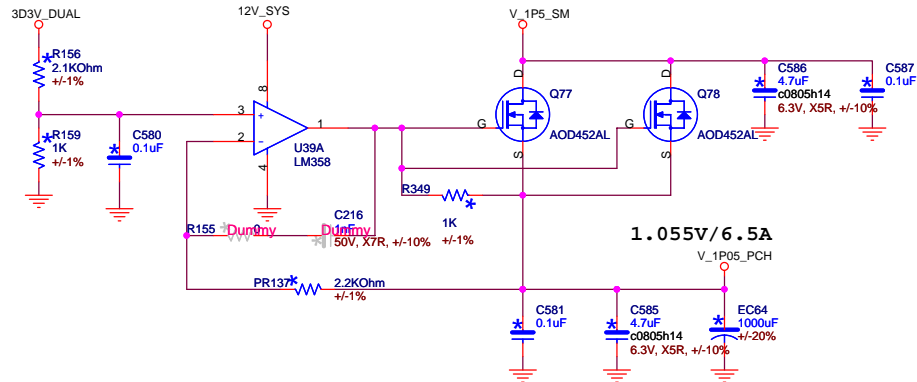
Title

ATX CONN/RESUME RESET

Size A3 Document Number H55MXV Rev 500

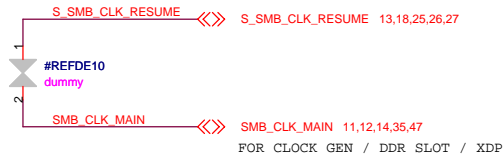
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+V_1.05_PCH

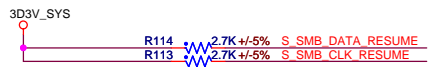
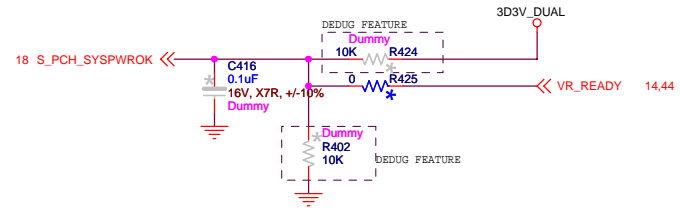


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SMB ISOLATE



VR_READY DEFENSIVE (PCH POWEROK)



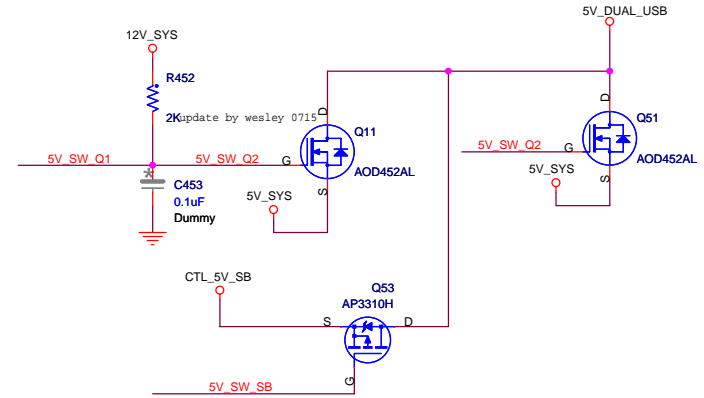
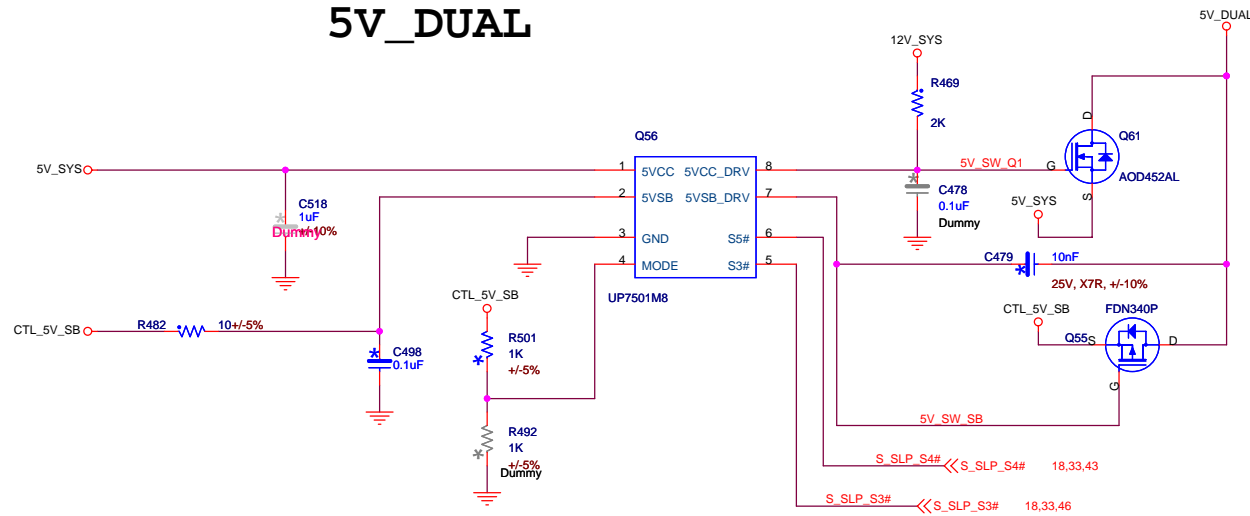
FOXCONN PCEG

Title	POWER-1:LINEAR POWER-1
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5V_DUAL

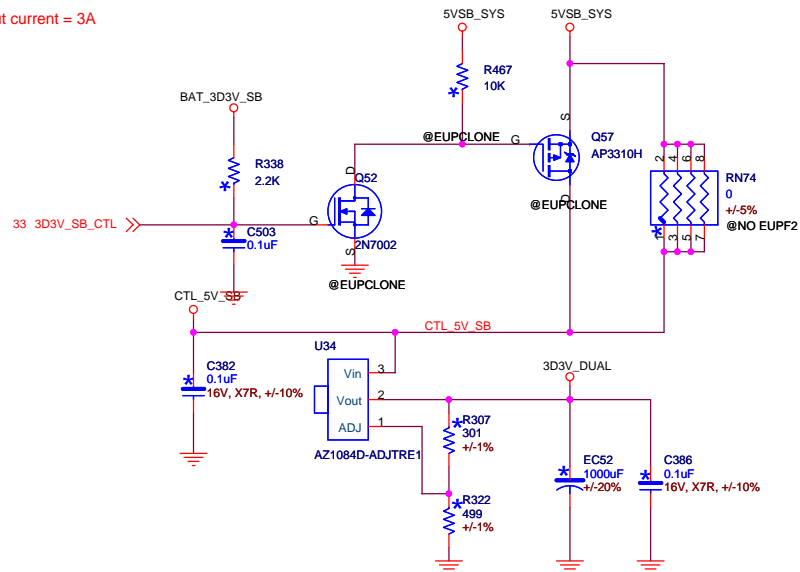


HI= S4/S5 5VDUAL FORM 5VSB
Low= S4/S5 5VDUAL TURN OFF

S5	S3	NODE	5VDUAL
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

3D3V_SB

Max. output current = 3A



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

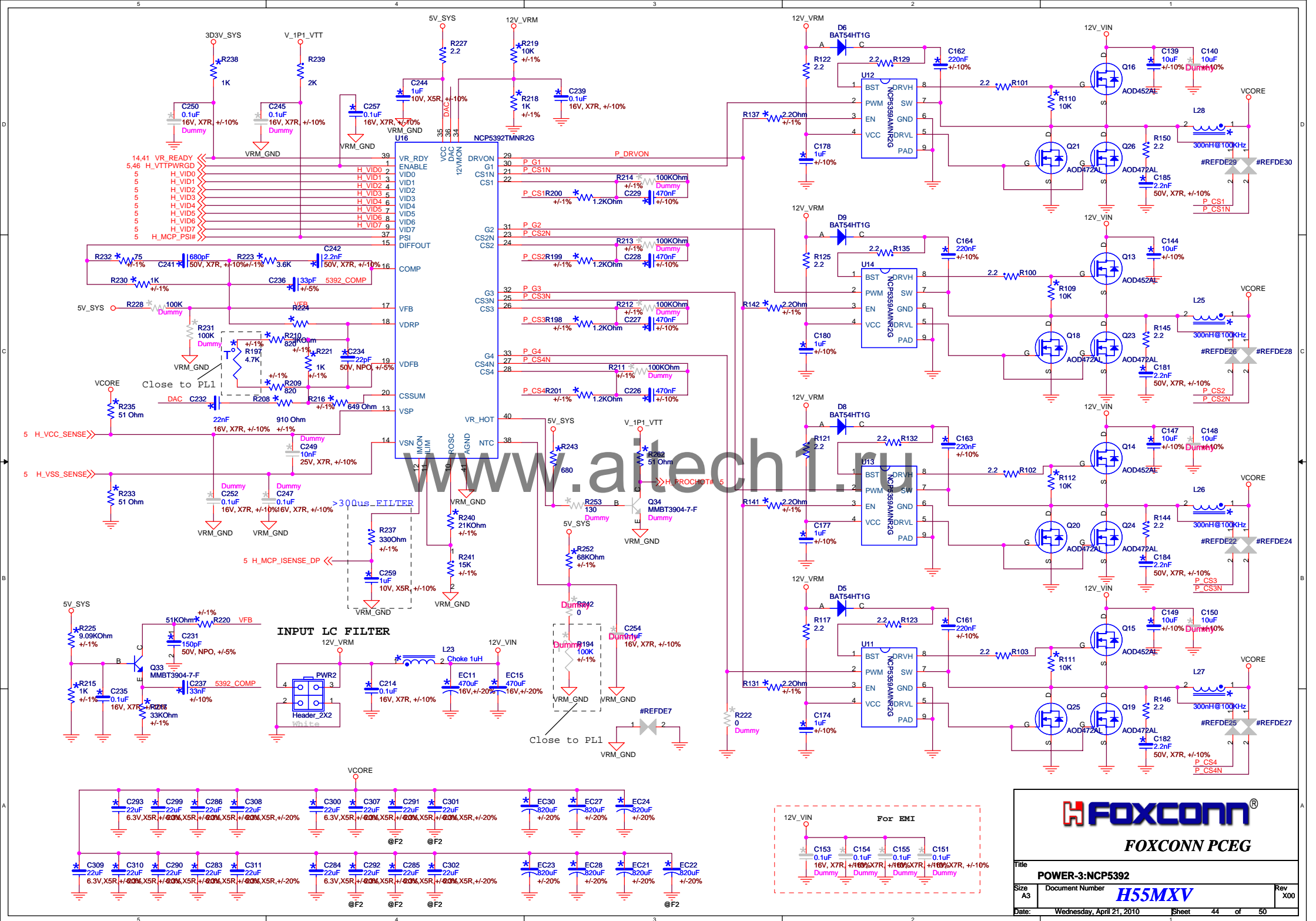


FOXCONN PCEG

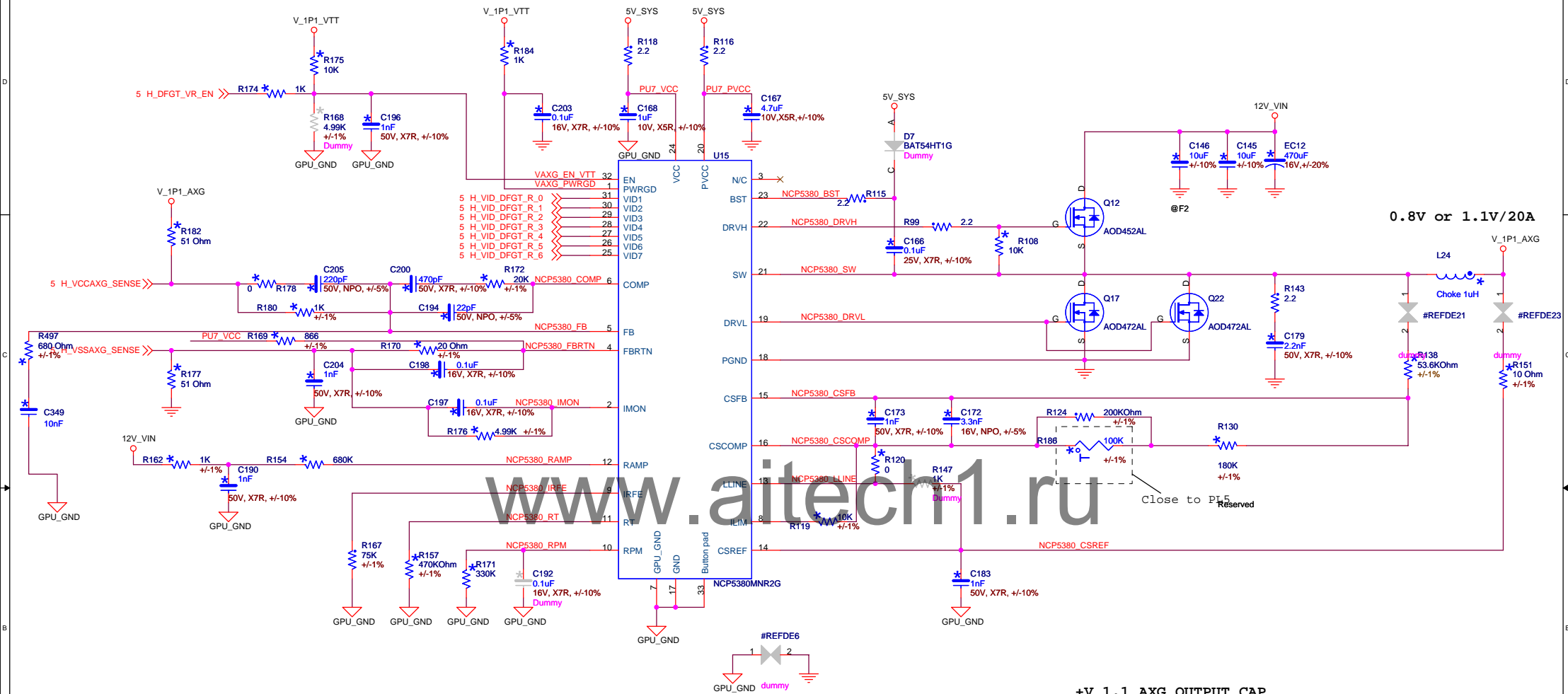
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Size A3	Document Number H55MXV
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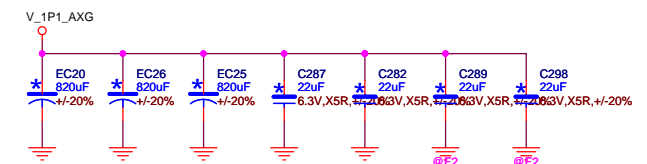
Date: Wednesday, April 21, 2010 Sheet 42 of 50



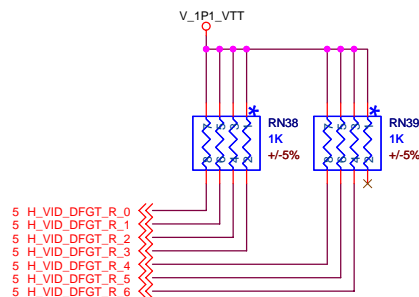
+V_1.1_AXG



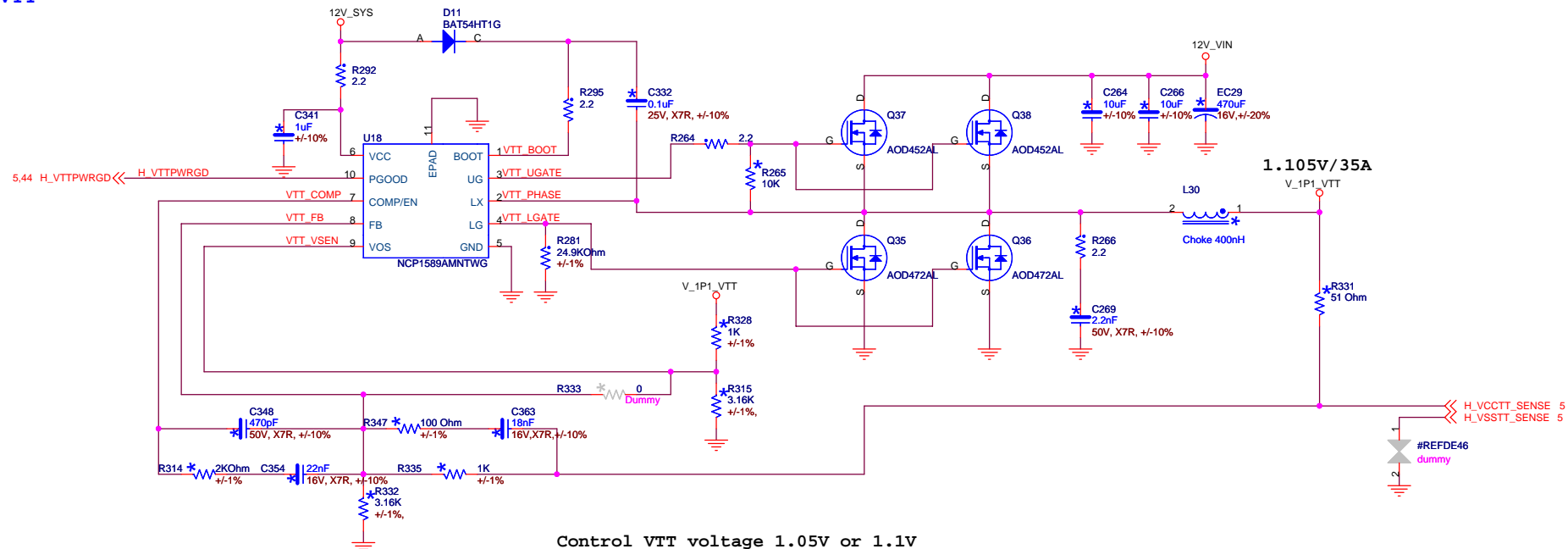
+V_1.1_AXG OUTPUT CAP



Intel Demo board 1.0	
H_VID_DFGT_R_0	L
H_VID_DFGT_R_1	Floating
H_VID_DFGT_R_2	Floating
H_VID_DFGT_R_3	Floating
H_VID_DFGT_R_4	Floating
H_VID_DFGT_R_5	Floating
H_VID_DFGT_R_6	H
H_VID_DFGT_R_7	Floating

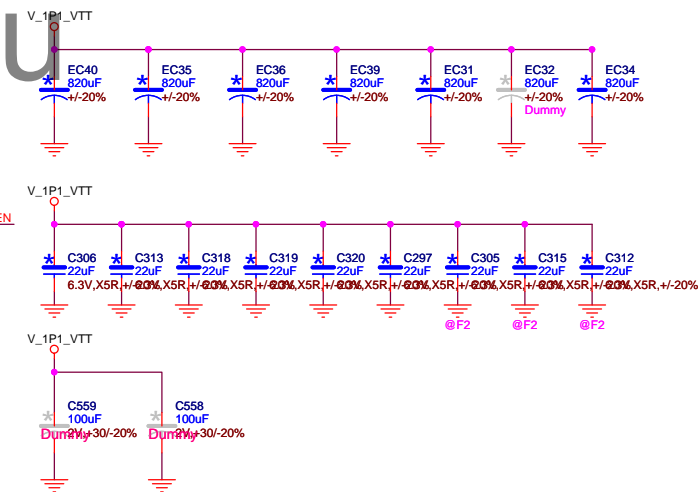


+V_1.1_VTT



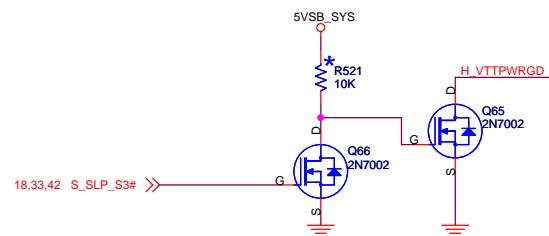
Control VTT voltage 1.05V or 1.1V

1.1V VTT OUTPUT CAP



+V_1.1_VTT Enable Circuit

+V_1.1_VTT Enable Circuit



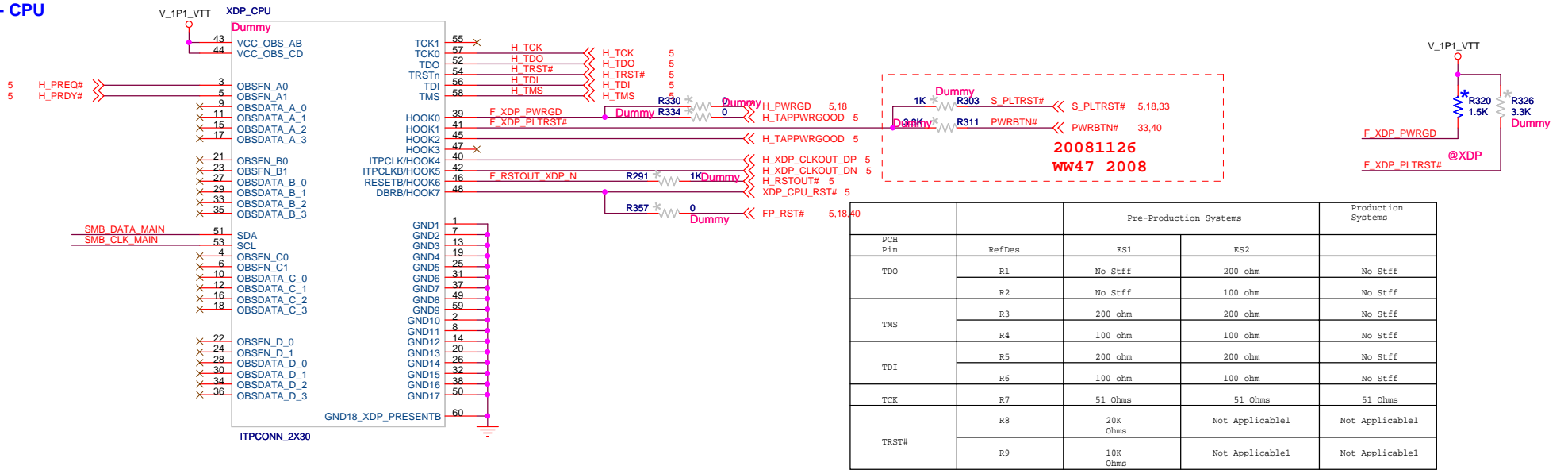
Enable Circuit for turn on/off Vcore



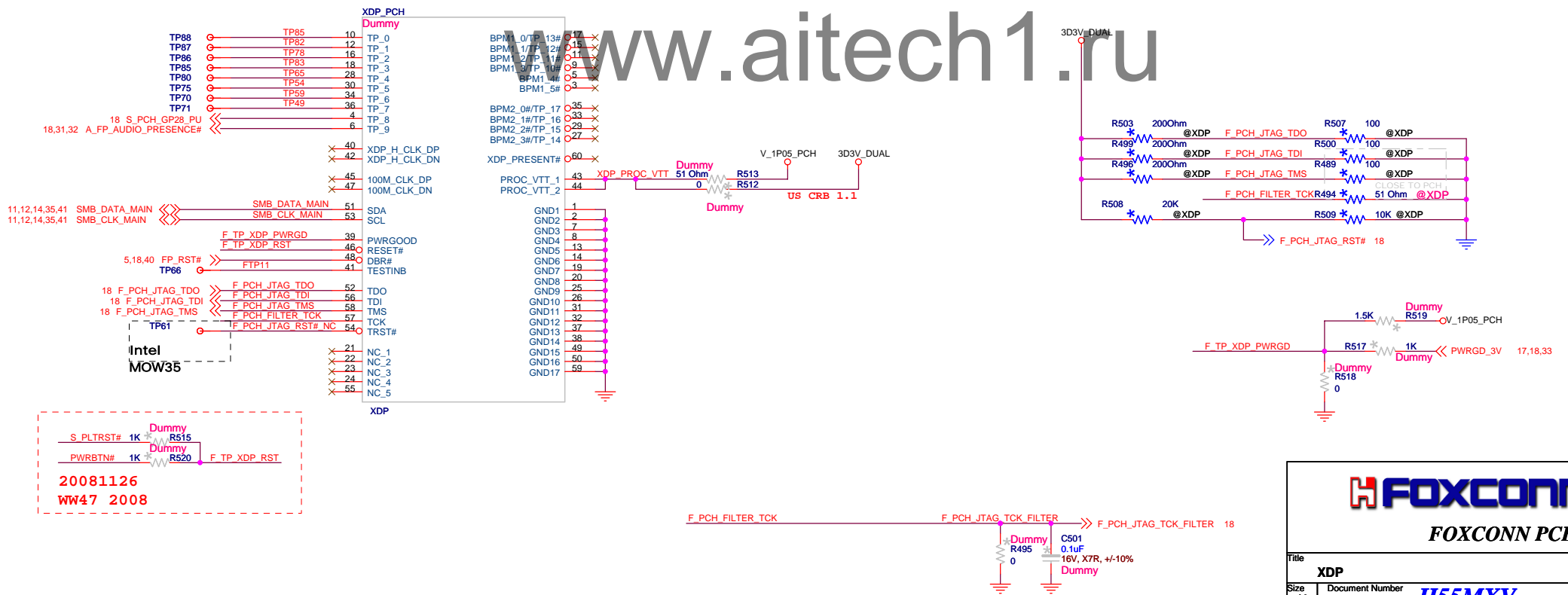
FOXCONN PCEG

Title			POWER-5:VTT
Size	A3	Document Number	H55MXV
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XDP Connector - CPU



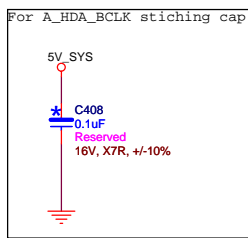
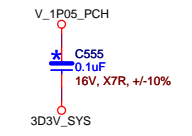
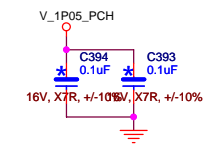
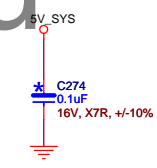
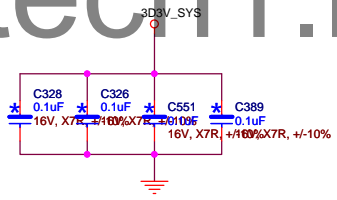
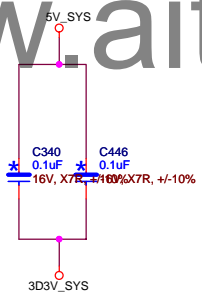
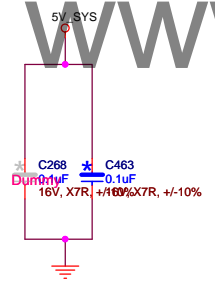
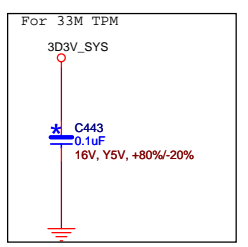
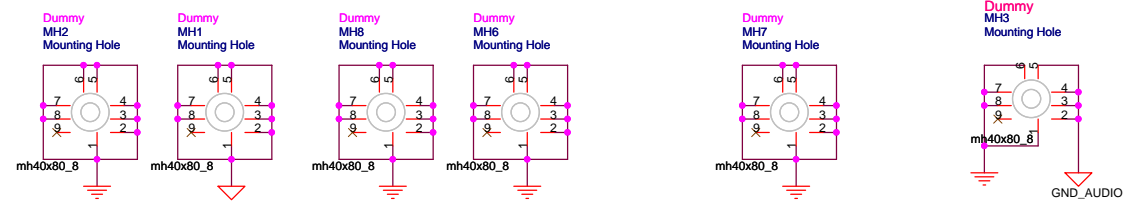
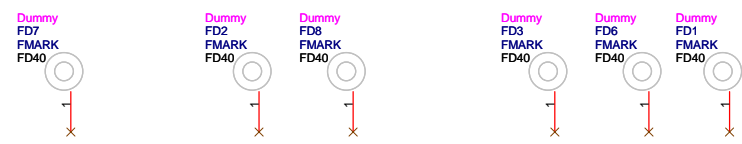
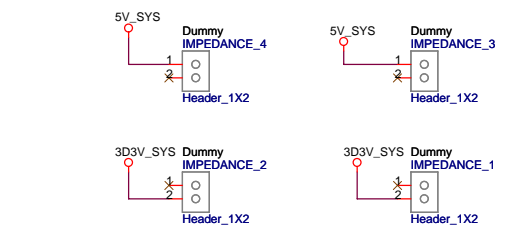
XDP Connector - PCH



FOXCONN PCEG

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Name	Type	Recommendations	Tolerance	Power Well	Default	Blink Capability	Default	Power Plane	During Reset4	Immediately after Reset4	S0/S1	S3	S4/S5
GPIO0	I/O	Multiplexed with EMBUSY#.	3.3 V	Core	GP1	Yes	TBD						
GPIO1	I/O	Multiplexed with TACH1.	3.3 V	Core	GP1	Yes	TBD						
GPIO2	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GP1	Yes	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO3	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GP1	Yes	TBD						
GPIO4	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GP1	Yes	TBD						
GPIO5	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GP1	Yes	TBD						
GPIO6	I/O	Multiplexed with TACH[3:2].	3.3 V	Core	GP1	Yes	TBD						
GPIO7	I/O	Multiplexed with TACH[3:2].	3.3 V	Core	GP1	Yes	TBD						
GPIO8 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	High	High	Defined	Defined	Defined
GPIO9	I/O	Multiplexed with OC5#	3.3 V	Suspend	Native	Yes	TBD						
GPIO10	I/O	Multiplexed with OC6#	3.3 V	Suspend	Native	Yes	TBD						
GPIO11	I/O	Multiplexed with SNEALERT#.	3.3 V	Suspend	Native	Yes	TBD						
GPIO12	I/O	Multiplexed with LAN_PHY_PWR_CTRL. GPIO / Native functionality controlled via soft strap	3.3 V	Suspend	GP1	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO13	I/O	Multiplexed with HDA_DOCK_RST# (Mobile Only)	3.3 V	Suspend	GP1	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO14	I/O	Multiplexed with OC7#	3.3 V	Suspend	Native	Yes	TBD						
GPIO15 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO16	I/O	Multiplexed with SATA4GP.	3.3 V	Core	GP1	Yes	TBD						
GPIO17	I/O	Multiplexed with TACH0.	3.3 V	Core	GP1	Yes	TBD						
GPIO18	I/O	Multiplexed with PCIECLKRQ1#	3.3 V	Core	Native	Yes	TBD						
GPIO19	I/O	Multiplexed with SATA1GP	3.3 V	Core	GP1	Yes	TBD						
GPIO20	I/O	Multiplexed with PCIECLKRQ2#	3.3 V	Core	Native	Yes	TBD						
GPIO21	I/O	Multiplexed with SATA0GP	3.3 V	Core	GP1	Yes	TBD						
GPIO22	I/O	Multiplexed with SLOCK	3.3 V	Core	GP1	Yes	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO23	I/O	Multiplexed with LDRQ1#.	3.3 V	Core	Native	Yes	TBD						
GPIO24	I/O	Unmultiplexed NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO25	I/O	Multiplexed with PCIECLKRQ3#	3.3 V	Suspend	Native	Yes	TBD						
GPIO26	I/O	Multiplexed with PCIECLKRQ4#	3.3 V	Suspend	Native	Yes	TBD						
GPIO27 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO28	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO29	I/O	Multiplexed with SLP_LAN#	3.3 V	Suspend	GP1	No	TBD	Suspend	High-Z	High-Z	High	Defined	Defined
GPIO30	I/O	Multiplexed with SUS_PWR_DN_ACK Desktop: Cannot be used for native function. Used as GPIO30 only. Mobile: Used as SUS_PWR_DN_ACK or GPIO30	3.3 V	Suspend	GP1	Yes	TBD	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO31	I/O	Multiplexed with ACPRESENT	3.3 V	Suspend	GP1	Yes	TBD	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined

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Name	Type	Recommendations	Tolerance	Power Well	Default	Blink Capability	Default	Power Plane	During Reset4	Immediately after Reset4	S0/S1	S3	S4/S5
GPIO32	I/O	Unmultiplexed	3.3 V	Core	GPO	No	TBD	Core	High	High	Defined	Off	Off
GPIO33 (Strapping)	I/O	Multiplexed with HDA_DOCK_EN# (Mobile Only)	3.3 V	Core	GPO	No	TBD	Core	High	High	Defined	Off	Off
GPIO34	I/O	Multiplexed with STP_PCI#	3.3 V	Core	GP1	No	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO35	I/O	Multiplexed with SATACLKREQ#.	3.3 V	Core	GPO	No	TBD	Core	Low	Low	Defined	Off	Off
GPIO 36	I/O	Multiplexed with SATA2GP.	3.3 V	Core	GP1	No	TBD						
GPIO 37	I/O	Multiplexed with SATA3GP.	3.3 V	Core	GP1	No	TBD						
GPIO38	I/O	Multiplexed with SLOAD.	3.3 V	Core	GP1	No	TBD	Core	High-Z (Input)	High-Z (Input)	Blinking	Off	Off
GPIO39	I/O	Multiplexed with SDATAOUT0.	3.3 V	Core	GP1	No	TBD	Core	High-Z	High-Z	High-Z	Off	Off
GPIO40	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO41	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO42	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO43	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO44	I/O	Multiplexed with PCIECLKRQ5#	3.3V	Suspend	Native	No	TBD						
GPIO45	I/O	Multiplexed with PCIECLKRQ6#	3.3V	Suspend	Native	No	TBD						
GPIO46	I/O	Multiplexed with PCIECLKRQ7#	3.3V	Suspend	Native	No	TBD						
GPIO47	I/O	Multiplexed with PEG_A_CLKRQ#	3.3V	Suspend	Native	No	TBD						
GPIO48	I/O	Multiplexed with SDATAOUT1.	3.3 V	Core	GP1	No	TBD	Core	High-Z	High-Z	High-Z	Off	Off
GPIO49	I/O	Multiplexed with SATA5GP	3.3V	Core	GP1	No	TBD						
GPIO50	I/O	Multiplexed with REQ1#.	5.0 V	Core	Native	No	TBD						
GPIO51 (Strapping)	I/O	Multiplexed with CNT1#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO52	I/O	Multiplexed with REQ2#.	5.0 V	Core	Native	No	TBD						
GPIO53	I/O	Multiplexed with CNT2#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO54	I/O	Multiplexed with REQ3#.	5.0 V	Core	Native	No	TBD						
GPIO55	I/O	Multiplexed with CNT3#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO56	I/O	Multiplexed with PEG_B_CLKRQ#	3.3 V	Suspend	Native	No	TBD						
GPIO57	I/O	Unmultiplexed	3.3 V	Suspend	GP1	No	TBD	Suspend	High-Z (Input)	High-Z (Input)	Driven	Driven	Driven
GPIO58	I/O	Multiplexed with SMLCLK	3.3 V	Suspend	Native	No	TBD	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO59	I/O	Multiplexed with OC[0]#	3.3 V	Suspend	Native	No	TBD						
GPIO60	I/O	Multiplexed with SML0ALERT#	3.3 V	Suspend	Native	No	TBD	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO61	I/O	Multiplexed with SUS_STAT#	3.3 V	Suspend	Native	No	TBD	Suspend	Low	High	High	Low	Low
GPIO62	I/O	Multiplexed with SUSCLK	3.3 V	Suspend	Native	No	TBD	Suspend	Low	Running	Running	Running	Running
GPIO63	I/O	Multiplexed with SLP_S5#	3.3 V	Suspend	Native	No	TBD	Suspend	Low	High	High	High	Low3
GPIO64	I/O	Multiplexed with CLKOUTFLEX0	3.3 V	Core	Native	No	H	Core	Running	Running	Running	Off	Off
GPIO65 (Strapping)	I/O	Multiplexed with CLKOUTFLEX1	3.3 V	Core	Native	No	H	Core	Running	Running	Running	Off	Off
GPIO66	I/O	Multiplexed with CLKOUTFLEX2	3.3 V	Core	Native	No	L	Core	Running	Running	Running	Off	Off
GPIO67	I/O	Multiplexed with CLKOUTFLEX3	3.3 V	Core	Native	No	L	Core	Running	Running	Running	Off	Off
GPIO72	I/O	Mobile: Multiplexed with BATLOW#. Desktop: Unmultiplexed	3.3 V	Suspend	Native	No	H	Suspend	High-Z (Input)	High-Z (Input)	Driven	Driven	Driven
GPIO73	I/O	Multiplexed with PCIECLKRQ0#	3.3 V	Suspend	Native	No	H						
GPIO74	I/O	Multiplexed with SML1ALERT#	3.3 V	Suspend	Native	No	H	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO75	I/O	Multiplexed with SML1DATA	3.3 V	Suspend	Native	No	H	Suspend	High-Z	High-Z	Defined	Defined	Defined



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Changelist:

- 1. LAN Power
- 2. change VGA HYSN and VYSN's buffer package type
- 3.change clr header/s pin definition
- 4. change IR/CIR to CIR/change PCIE_1X and COM2 'S Sybol name
- 5. change EC64 , EC65 and C371'S footprint
- 6. add C503 near Q52
- 7.connect SIO susc pin to SLP_S4#

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